Curriculum Vitae

Scott C. Karlin

Department of Computer Science
Princeton University
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EDUCATION:

PhD, Computer Science — January 2003
Princeton University, Princeton, NJ
Advisor: Larry Peterson
Thesis: "Embedded Computational Elements in Extensible Routers."

MS, Computer Science — May 1994
Loyola Marymount University, Los Angeles, CA

BS, Electrical Engineering — June 1986
California Institute of Technology, Pasadena, CA

PROFESSIONAL EXPERIENCE:

Senior Manager, Computing Facilities — January 2013 – present
Manager, Computing Facilities — October 2004 – December 2012
Princeton University Computer Science Department, Princeton, NJ

- Manage the group that installs, maintains, and upgrades the computing and networking infrastructure as well as develops and deploys applications for the department-wide academic, research, and administrative needs of the department.
- Develop and maintain software supporting academic courses, departmental student records, and internal billing.
- Represent the department on various standing and *ad hoc* committees relating to technology and policy.

Consultant — September 2003 – present
Karlin Consulting, LLC, Plainsboro, NJ

- Served as expert for Petitioners EMC Corp. and Lenovo US Corp. in 1:16–cv–10860–PBS, which successfully challenged the assertion of infringement of claims 15, 18, 24, and 25 of US 6,968,459, 2019–2020.
- Served as expert for Petitioners EMC Corp. and Lenovo US Corp. in IPR2017–00477, which successfully challenged the patentability of claims 1 and 9 of US 8,387,132 B2, 2016–2018.
- Web development (Django, Python, PostgreSQL) for pharma news aggregation startup, 2015–present.
- Non-testifying technology expert for dispute related to APIs for electronic medical record and billing software, 2012.
- FXO Inc.: satellite test software development, 2003 and 2008-2009; tsunami sensor development, 2007.
- Technology consultant for local performing arts organizations, 2003–present.

Lecturer — spring 2016, fall 2020
Teaching Assistant — September 1996 – June 2008
Princeton University Computer Science Department, Princeton, NJ

- COS 217, Introduction to Programming Systems: fall 1998, spring 2016, fall 2020
- COS 126, General Computer Science: spring 1997, spring 2008
- COS 471, Computer Architecture and Organization: fall 1996

Research Staff November 2003 – September 2004
Postdoctoral Research Associate November 2002 – October 2003
Graduate Student September 1996 – October 2002
Research Staff June 1996 – August 1996
Princeton University Computer Science Department, Princeton, NJ

- Researcher for PlanetLab (www.planet-lab.org), a global testbed for developing, deploying, and accessing new planetary-scale network services.
- Researcher in the Network Systems Group. Designed and developed key portions of an extensible router using line cards based on Intel IXP1200 network processors and embedded PowerPC processors.
- Researcher for the SHRIMP Project. Designed and supervised the fabrication of the SurfBoard, a custom hardware performance monitor for the SHRIMP system.

Summer Technical Staff / Consultant June 1998 – September 1999
Sarnoff Corporation, Princeton, NJ

- Research in FPGA based network packet processing. Developed portions of runtime hardware library in VHDL for a C-like language compiler for a hybrid FPGA/processor system.

Manager, Real-Time Data Systems March 1995 – May 1996
Information Management Group, Nicholas Applegate Capital Management, San Diego, CA

- Responsible for real-time data feeds which provide stock prices to the entire firm. Included architecture design, reliabilty analysis, vendor interaction, and software development to integrate various off-the-shelf systems on SunOS, Solaris, and NEXTSTEP environments.

Project Engineer August 1986 – March 1995
Data Technologies Division, TRW, Redondo Beach, CA

- Principal Investigator for an R&D project to design systems for processing frequency-agile signals.
- Associate Principal Investigator for an R&D project to develop a parallel processing architecture using the High-Performance Parallel Interface (HIPPI) to connect multiple VME card cages.
- Instructor for the internal *Programming in "C" for Software Engineers* course. The course consisted of Twelve 2 hour classes.
- Software engineer for heterogeneous multiprocessor VMEbus based system using i860 and 680x0 based CPUs. Designed, implemented, and tested a Designed and implemented a subsystem which used multiple processors to perform bit, frame, and block synchronization as well as BCH error correction on a high-speed data stream in real-time. Developed a portable, real-time kernel, interprocessor communication library, and operating environment.

Member of the Technical Staff summer 1982, 1983, 1985, 1986
The Aerospace Corporation, El Segundo, CA part time 1981–82

- Installed a commercial hypercubic concurrent processor and instructed employees in its use.
- Design of tracking algorithms using cellular logic for systolic processing architectures. Presented formal seminar on concurrent processing. Developed software for image processing and graphics applications.

TECHNICAL INTERESTS:

My technical interests primarily lie near the interface between the hardware and the software in computer systems. I'm specifically interested in operating systems, networking, security & privacy (and related policy), embedded systems, Internet-of-Things (IoT), and home automation.

PROFESSIONAL SERVICE:

Program Committee member and Webmaster for *OPENARCH 2002*, the Fifth IEEE Conference on Open Architectures and Network Programming, June 2002.
Program Committee member for *OPENARCH 2003*, the Sixth IEEE Conference on Open Architectures and Network Programming, April 2003.

UNIVERSITY SERVICE:

Data Center Advisory Group, 2012–present
Research Computing Advisory Group, 2004–present
Controlled Unclassified Information (NIST 800–171) Working Group, 2018–2020
Princeton Application Developers, steering committee, 2008–2015
Computer Security Team, 2006–2012

AWARDS:

Intel Foundation Graduate Fellowship for academic year 1999–2000.
Princeton University Engineering Council Award for Excellence in Teaching, for COS 217, fall 1998.

CERTIFICATIONS:

ITIL Foundation v3, December 2009

PAPERS:

A. Bavier, M. Bowman, D. Culler, B. Chun, S. Karlin, S. Muir, L. Peterson, T. Roscoe, T. Spalink, M. Wawrzoniak. Operating System Support for Planetary-Scale Network Services. In *Proceedings of the First Symposium on Network Systems Design and Implementation (NSDI),* March 2004. Winner of a 2014 USENIX Test of Time Award.

S. Karlin, L. Peterson. VERA: An Extensible Router Architecture. *Computer Networks,* 38(3):277–293, February 2002. An earlier version appears in the *Proceedings of the 4th International Conference on Open Architectures and Network Programming (OPENARCH)*, pages 3–14, Anchorage, Alaska, April 2001.

N. Shalaby, L. Peterson, A. Bavier, Y. Gottlieb, S. Karlin, A. Nakao, X. Qie, T. Spalink, M. Wawrzoniak. Extensible Routers for Active Networks. In *Proceedings of the DARPA Active Networks Conference and Exposition*, pages 92–116, San Francisco, California, May 2002.

S. Karlin, L. Peterson. Maximum Packet Rates for Full-Duplex Ethernet. Technical Report TR–645–02, Princeton University, Princeton, New Jersey, February 2002.

T. Spalink, S. Karlin, L. Peterson, Y. Gottlieb. Building a Robust Software-Based Router Using Network Processors. In *Proceedings of the 18th ACM Symposium on Operating Systems Principles (SOSP)*, pages 216–229, Chateau Lake Louise, Banff, Alberta, Canada, October 2001.

X. Qie, A. Bavier, L. Peterson, S. Karlin. Scheduling Computations on a Programmable Router. In *Proceedings of the ACM SIGMETRICS 2001 Conference*, pages 13–24, Cambridge, Massachusetts, June 2001.

T. Spalink, S. Karlin, L. Peterson. Evaluating Network Processors in IP Forwarding. Technical Report TR–626–00, Princeton University, Princeton, New Jersey, November 2000.

L. Peterson, S. Karlin, K. Li. OS Support for General-Purpose Routers. In *Proceedings of the 7th Workshop on Hot Topics in Operating Systems (HotOS–VII)*, pages 38–43, Rio Rico, Arizona, March 1999.

S. Karlin, D. Clark, M. Martonosi, SurfBoard – A Hardware Performance Monitor for SHRIMP. Technical Report TR–596–99, Princeton University, Princeton, New Jersey, March 1999.

M. Martonosi, S. Karlin, C. Liao, D. Clark. Performance Monitoring Infrastructure in Shrimp Multicomputers. *International Journal of Parallel and Distributed Systems and Networks (Invited paper in the special issue on Measurement of Program and System Performance)*, 2(3):126–133, 1999.

E. Felten, S. Karlin, S. Otto. The Traveling Salesman Problem on a Hypercubic, MIMD Computer. In *Proceedings of the 1985 International Conference on Parallel Processing*, pages 6–10, St. Charles, Illinois, August 1985.

E. Felten, S. Karlin, S. Otto. Sorting on a Hypercubic, MIMD Computer. Technical Report HM92B, Caltech Concurrent Computation Project, California Institute of Technology, Pasadena, California, 1985.