Hansen Zhang

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EDUCATION

Princeton University, Princeton, NJ **Expected May 2019**
Ph.D. Candidate in Computer Science, GPA 3.76
Advisor: Prof. David August
Princeton University Graduate Fellowship, 2014 – 2015

Boston University, Boston, MA **2012 - 2014**
Master of Science in Computer Engineering, GPA 3.96

RESEARCH PROJECTS

Liberty Research Group at Princeton University, Research Assistant **2014 - Present**

- Design a novel security architecture for privacy protection via instruction-grained run-time monitoring
- Implement a cache mirroring scheme to optimize performance and achieved 80% reduction in performance overhead while reducing architectural complexity
- Prototype the security architecture on NetFPGA based on the open source RISC-V architecture with < 10% performance overhead

CAAD Lab at Boston University, Master's Thesis **2013 - 2014**

- Designed and implemented singlenode/multinode FPGA system architecture for 3D FFT computation
- Achieved average speedup of 2x over GPU and 10x over CPU for various problem sizes on a single FPGA
- Validated the design against Matlab model, with relative difference less than 0.008%

WORK EXPERIENCE

Microsoft Research **Summer 2018**
Research Intern, Catapult Team **Redmond, WA**

- Worked on building FPGA-based Hardware Security Module for Microsoft's Cloud Platform
- Implemented TCP/IP, TLS and HTTPS stacks on Altera Nios II Processor
- Co-authored provisioning protocol for establishing trust in cloud-based Hardware Security Modules
- Designed Hardware Cryptographic IP with encryption/decryption throughput of 24Gb/s

MediaTek USA Inc. **Summer 2014**
Research Intern **Woburn, MA**

- Designed simulated annealing based algorithm that optimizes memory allocation for area, utilization and load balancing
- Implemented automated system for translating user defined constraints and trace generated constraints into optimized program specifications
- Augmented constraint based model by doubling the amount of user defined allocation rules

PUBLICATIONS

Hardware Trust via Containment
Zhang, H., Ghosh, S., Fix, J., Apostolakis, S., Beard, S., Nagendra, N., Oh, T., August, D., *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2019 IEEE

Hardware Multithreaded Transactions
Fix, J., Nagendra, N., Apostolakis, S., Zhang, H., Qiu, S., August, D., *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2018 IEEE, March 2018

3D FFTs on a Single FPGA
Humpries, B., Zhang, H., Sheng, J., Landaverde, R., and Herbordt, M., *Field-Programmable Custom Computing Machines (FCCM)*, 2014 IEEE, May 2014

Design of 3D FFTs with FPGA Clusters
Sheng, J., Humpries, B., Zhang, H., and Herbordt, M., *High Performance Extreme Computing Conference (HPEC)*, 2014 IEEE, September 2014

TECHNICAL SKILLS

- **Programming languages**: Java, Verilog, C/C++, Python, Objective-C, HTML, JavaScript, Assembly

TEACHING EXPERIENCE

COS126 – Computer Science: An Interdisciplinary Approach	Spring 2017, Princeton University
COS217 - Introduction to Programming Systems	Fall 2016, Princeton University
COS333 - Advanced Programming Techniques	Spring 2016, Princeton University
COS/ELE375 - Computer Architecture and Organization	Fall 2015, Princeton University
EC527 - High Performance Programming with Multicore and GPUs	Spring 2014, Boston University
EC513 - Computer Architecture	Fall 2013, Boston University

COURSE PROJECT

Project: Dynamic Learning Rate Adjustment Algorithm **Spring 2015**
Course: Advanced Algorithm Design

- Designed an online gradient descent algorithm with dynamically adjusted learning rate for portfolio management
- Tested the profitability of the algorithm on a variety of long-term daily-resolution stock data sets from across the world

Project: Interacting with Piano **Spring 2015**
Course: Fundamentals of Machine Learning

- Implemented machine learning algorithms to perform automatic real-time music pitch detection
- Evaluated multiple classification methods in terms of performance and precision
- Designed an aggregated classifier for better noise resistance in real-world environment

Project: Stencil Computation Optimization **Spring 2013**
Course: High Performance Programming with Multicore and GPUs

- Experimented with a 7-point stencil and perform optimization on different platforms including single core CPU, multiple core CPU and NVidia GPGPU
- Tested optimization methods including blocking, unrolling, reordering and prefetching and the use of shared memory and memory coalescing on the GPU architecture

Project: FPGA-based Arcade Game: 'Battle City' **Fall 2012**
Course: Advanced Digital Design with Verilog and FPGA

- Implemented the game on the Spartan6 FPGA, with external PS2 keyboard and VGA monitor
- Designed gaming graphics including two background maps, one for each level of the game