Hansen Zhang

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EDUCATION

Princeton University Computer Science Department, Princeton, NJ **Expected May 2019**
Ph.D. Candidate in Computer Science
Advisor: Prof. David August
Princeton University Graduate Fellowship, 2014 – 2015

Boston University College of Engineering, Boston, MA **May 2014**
Master of Science in Computer Engineering

Fudan University School of Information, Shanghai, China **June 2012**
Bachelor of Science in Electronic Engineering

RESEARCH PROJECTS

Research Assistant **September 2014 – Present**
Liberty Research Group at Princeton University **Princeton, NJ**

- Design a novel security architecture that leverages parallelism to perform instruction-grained run-time monitoring
- Implement a cache mirroring scheme to optimize performance and achieved 80% reduction in performance overhead while reducing architectural complexity
- Use a Merkle tree based algorithm to protect the integrity of data in the system against replay attacks
- Prototype the security architecture on FPGA based on the open source RISC-V architecture

Master's Thesis **September 2013 – May 2014**
CAAD Lab at Boston University **Boston, MA**

- Designed and implemented singlenode/multinode FPGA system architecture for 3D FFT computation
- Achieved average speedup of 2x over GPU and 10x over CPU for various problem sizes on a single FPGA
- Validated the design against Matlab model, with relative difference less than 0.008%

PUBLICATIONS

Ghosh, S., Zhang, H., Fix, J., Apostolakis, S., Beard, S., Nagendra, N., Oh, T., August, D. "TrustGuard: Containment Architecture with Verified Output", In preparation for submission

Fix, J., Nagendra, N., Apostolakis, S., Zhang, H., Qiu, S., August, D. "Hardware Multithreaded Transactions", To appear in *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2018 IEEE, March 2018

Humpries, B., Zhang, H., Sheng, J., Landaverde, R., and Herbordt, M. "3D FFTs on a Single FPGA", *Field-Programmable Custom Computing Machines (FCCM)*, 2014 IEEE, May 2014

Sheng, J., Humpries, B., Zhang, H., and Herbordt, M. "Design of 3D FFTs with FPGA Clusters", *High Performance Extreme Computing Conference (HPEC)*, 2014 IEEE, September 2014

WORK EXPERIENCE

Summer Intern **May 2014 – August 2014**
Mediatek, Inc **Woburn, MA**

- Designed simulated annealing based algorithm that optimizes memory allocation for area, utilization and load balancing for Mediatek's LTE chipset
- Implemented automated system for translating user defined constraints and trace generated constraints into optimized program specifications
- Augmented constraint based model by doubling the amount of user defined allocation rules

TECHNICAL SKILLS

- **Programming languages**: Java, Verilog, C/C++, Python, Objective-C, HTML, JavaScript, Assembly

TEACHING EXPERIENCE

COS126 – Computer Science: An Interdisciplinary Approach — Spring 2017, Princeton University
COS217 - Introduction to Programming Systems — Fall 2016, Princeton University
COS333 - Advanced Programming Techniques — Spring 2016, Princeton University
COS/ELE375 - Computer Architecture and Organization — Fall 2015, Princeton University
EC527 - High Performance Programming with Multicore and GPUs — Spring 2014, Boston University
EC513 - Computer Architecture — Fall 2013, Boston University

COURSE PROJECT

Project: Dynamic Learning Rate Adjustment Algorithm
Course: Advanced Algorithm Design **Spring 2015**

- Designed an online gradient descent algorithm with dynamically adjusted learning rate for portfolio management
- Tested the profitability of the algorithm on a variety of long-term daily-resolution stock data sets from across the world

Project: Interacting with Piano
Course: Fundamentals of Machine Learning **Spring 2015**

- Implemented machine learning algorithms to perform automatic real-time music pitch detection
- Evaluated multiple classification methods in terms of performance and precision
- Designed an aggregated classifier for better noise resistance in real-world environment

Project: Stencil Computation Optimization
Course: High Performance Programming with Multicore and GPUs **Spring 2013**

- Experimented with a 7-point stencil and perform optimization on different platforms including single core CPU, multiple core CPU and NVidia GPGPU
- Tested optimization methods including blocking, unrolling, reordering and prefetching and the use of shared memory and memory coalescing on the GPU architecture

Project: FPGA-based Arcade Game: 'Battle City'
Course: Advanced Digital Design with Verilog and FPGA **Fall 2012**

- Implemented the game on the Spartan6 FPGA, with external PS2 keyboard and VGA monitor
- Designed gaming graphics including two background maps, one for each level of the game