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## Education

Ph.D. in Computer Science, Carnegie-Mellon University, 1976
Xerox Graduate Fellow, 1973–1976

B.S. *magna cum laude* in Engineering and Applied Science, Yale University, 1972
Yale National Scholar, 1968–1972

## Employment

Professor of Computer Science
Princeton University, since 1993

Visiting Professor of Computer and Information Science
University of Pennsylvania, spring 2003

Senior Consulting Engineer
Alpha Advanced Development, Digital Equipment Corp., 1991–1993

Visiting Lecturer
Division of Applied Sciences, Harvard University, 1990–1991

Consulting Engineer, then Senior Consulting Engineer
Advanced VAX Systems Engineering, Digital Equipment Corp., 1982–1990

Principal Engineer
Systems Architecture Group, Digital Equipment Corp., 1980–1982

Member of the Research Staff
Computer Science Laboratory, Xerox Palo Alto Research Center, 1976–1980

## Professional activities

International Conference on Computer Design: program committee member, 2003

SIGMETRICS Conference on Measurement and Modeling of Computer Systems: program committee member, 1998, 1991, 1990

NSF Workshop on Critical Issues in Computer Architecture Research: workshop organizer, May 1996

Conference on Architectural Support for Programming Languages and Operating Systems: program chair, 1994; program committee member, 1992, 1988, 1982

*ACM Transactions on Computer Systems*: associate editor, 1983–1993

NSF Synthesis Engineering Education Coalition: national advisory committee member, 1990–1993

NSF Division of Microelectronic Information Processing Systems: advisory committee member, 1989–1992

International Symposium on Computer Architecture: program committee member, 1990, 1985; program committee co-chair, 1986

## Publications

Wu, Q. Reddi, V., Wu, Y. Lee, J., Connors, D., Brooks, D., Martonosi, M., and Clark, D.W. "Dynamic Compiler Driven Control for Microprocessor Energy and Performance," *IEEE Micro* Special Issue: Top Picks from Computer Architecture Conferences, Vol. 26, No. 1, Jan./Feb., 2006.

Wu, Q. Reddi, V., Wu, Y. Lee, J., Connors, D., Brooks, D., Martonosi, M., and Clark, D.W. "A Dynamic Compilation Framework for Controlling Microprocessor Energy and Performance," *Proc. 38th IEEE/ACM International Symposium on Microarchitecture* (MICRO-38), Barcelona, Spain, November 2005. Best Paper Award.

Wu, Q., Juang, P., Peh, L.-S., Martonosi, M. and Clark, D.W. "Formal Control Techniques for Power-Performance Management," *IEEE Micro*, Vol 25, No. 5, Sept./Oct. 2005.

Juang, P., Wu, Q., Peh, L.-S., Martonosi, M. and Clark, D.W. "Coordinated, Distributed, Formal Energy Management of Chip Multiprocessors," *Proc. International Symposium on Low Power Electronics and Design* (ISLPED-05), San Diego, Aug. 2005.

Wallace, G., Anshus, O.J., Bi, P., Chen, H., Chen, Y., Clark, D., Cook, P., Finkelstein, A., Funkhouser, T., Gupta, A., Hibbs, M., Li, K., Liu, Z., Samanta, R., Sukthankar, R., and Troyanskaya, O. "Tools and Applications for Large-Scale Display Walls," *IEEE Computer Graphics*, Vol. 25, No. 4, July/Aug. 2005.

Q. Wu, P. Juang, M. Martonosi, and D. W. Clark, "Voltage and Frequency Control with Adaptive Reaction Time in Multiple-Clock-Domain Processors," *Proc. 11th International Symposium on High-Performance Computer Architecture* (HPCA-11), San Francisco, Feb. 2005.

Wu, Q., Juang, P., Martonosi, M., and Clark, D.W. "Formal Online Methods for Voltage/Frequency Control in Multiple Clock Domain Microprocessors," *Proc. Eleventh Int. Conf. on Architectural Support for*

*Programming Languages and Operating Systems* (ASPLOS-XI), Boston, Oct. 2004.

Y. Zhou, Y., Wang, L., Clark, D.W., and K. Li. "Thread Scheduling for Out-of-Core Applications with a Memory Server," ch. 9, *Scalable Input/Output: Achieving System Balance*, Daniel A. Reed, ed. MIT Press, 2004, pp. 233–253.

Juang, P., Skadron, K., Martonosi, M., Hu, Z., Clark, D.W, Diodato, P., and Kaxiras, S. "Implementing Branch-Predictor Decay Using Quasi-Static Memory Cells," *ACM Transactions on Architecture and Code Optimization*, Vol. 1, No. 2, June 2004.

Wu, Q., Pyatakov, A., Spiridonov, A., Raman, E., Clark, D.W., and August, D. "Exposing Memory Access Regularities Using Object-Relative Memory Profiling," *Proc. Second Ann. IEEE/ACM Int. Symp. on Code Generation and Optimization (CGO 2004)*, San Jose, March 2004.

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Hu, Z., Juang, P., Skadron, K., Martonosi, M., and Clark, D.W. "Applying Decay Strategies to Branch Predictors for Leakage Energy Savings," *Proc. 2002 Int. Conf. on Computer Design (ICCD2002)*, Sept. 2002.

Hu, Z., Juang, P., Diodato, P., Kaxiras, S., Skadron, K., Martonosi, M., and Clark, D.W. "Managing Leakage for Transient Data: Decay and Quasi-Static 4T Memory Cells," *Proc. 2002 Int. Symp. on Low Power Electronics and Design (ISLPED 2002)*, Aug. 2002.

Chen, Y., Chen, H., Clark, D.W., Liu, Z., Wallace, G., and Li, K. "Software Environments for Cluster-Based Display Systems," *IEEE Int. Symp. on Cluster Computing and the Grid (CCGrid 2001)*, May 2001.

Chen, Y., Clark, D.W., Finkelstein, A., Housel, T., and Li, K. "Automatic Alignment Of High-Resolution Multi-Projector Displays Using An Un-Calibrated Camera," *IEEE Visualization 2000*, Salt Lake City, Oct. 2000.

Skadron, K., Martonosi, M., and Clark, D.W. "A Taxonomy of Branch Mispredictions, and Alloyed Prediction as a Robust Solution to Wrong-History Mispredictions," *Int. Conf. on Parallel Architectures and Compilation Techniques*, Philadelphia, Oct. 2000.

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Skadron, K., Martonosi, M., and Clark, D.W. "Speculative Updates of Local and Global Branch History: A Quantitative Analysis," *The Journal of Instruction Level Parallelism*, vol. 2, January 2000 (http://www.jilp.org/vol2).

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Zhou, Y., Wang, L., Clark, D.W., and Li, K. "Thread Scheduling for Out-of-Core Applications with Memory Server on Multicomputers," *Proc. 6th Workshop on I/O in Parallel and Distributed Systems*, Atlanta, May 1999.

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Ahuja, P.S., Skadron, K., Martonosi, M., and Clark, D.W. "Multipath Execution: Opportunities and Limits," *Proc. 12th International Conference on Supercomputing*, Melbourne, July 1998.

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