# Concurrent Separation Logic for Pipelined Parallelization

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**Abstract.** Recent innovations in automatic parallelizing compilers are showing impressive speedups on multicore processors using shared memory with asynchronous channels. We have formulated an operational semantics and proved sound a concurrent separation logic to reason about multithreaded programs that communicate asynchronously through channels and share memory. Our logic supports shared channel endpoints (multiple producers and consumers) and introduces *histories* to overcome limitations with local reasoning. We demonstrate how to transform a sequential proof into a parallelized proof that targets the output of the parallelizing optimization DSWP (Decoupled Software Pipelining).

## 1 Introduction

We have created an operational semantics and a concurrent separation logic (CSL) to reason about the correctness of programs that share memory and use buffered channels to synchronize processes. These channels can be used directly by the programmer or automatically by a parallelizing compiler and are not restricted to point-to-point communication; multiple producers and multiple consumers may asynchronously access a channel. We have proved our CSL sound with respect to the operational semantics. Furthermore, we demonstrate how certain proofs of correctness for a sequential program can be used to generate a related proof (that maintains the original specification) for the parallelized output of an optimization.

CSL [9] is an extension of separation logic (SL), which is an extension of Hoare logic. SL facilitates local reasoning about resources used by a program, so that when analyzing a region of code, we may assume that actions made by the rest of the program cannot interfere. This is encapsulated in the "frame rule" of SL. Similarly, CSL facilitates local reasoning about resources in a concurrent program so that we can analyze just one process while assuming that other processes cannot interfere. CSL has already been used to reason about programs that use critical sections and locks [9][6].

Our logic can be used in proofs about compilers. Leroy and others proved correct compilers for sequential programs; Hobor et al. outlined how such proofs can be extended to concurrent programs [8][6]. We have designed our logic to be capable of extending these certified compilers to handle programs that use channels. Proofs in our logic can also be used in proof-carrying code frameworks.

#### **1.1** Parallelizing transformations

A parallelizing compiler attempts to optimize a program by automatically partitioning sequential code into multiple threads. A classic example of this is the DOALL optimization, which parallelizes while-loops that have no loopcarried dependencies by distributing the iterations among multiple threads. While DOALL has had some success, particularly in scientific and numerical computing, it is common for programs to have loop-carried dependencies, thus many programs cannot benefit from DOALL.

Another optimization is DOACROSS, which can handle loop-carried dependencies. This optimization partitions iterations among several threads, but also transmits dependencies between the threads with the hope that there is a significant task within the loop that can overlap with other iterations regardless of the dependency. Figure 1a shows an example trace of a loop where each iteration is composed of tasks A and B; A and B both depend on A, but A and B do not depend on B. Because the dependencies are transmitted bidirectionally between threads, any latency in communication or an iteration stalling will cause the entire computation to stall. Therefore, DOACROSS often does not yield significant performance gains. Pipelined parallelism identifies code that

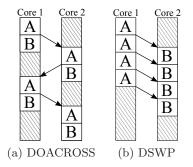


Fig. 1: Trace of DOACROSS vs. DSWP. Arrows depict data flow, control/data dependencies, and communication latency.

can be partitioned into tasks that have acyclic dependencies. Tasks that produce dependencies can run ahead of tasks that consume them, and tasks with no dependencies between them run in parallel. Such parallelism is often leveraged at the instruction level in hardware.

Decoupled Software Pipelining (DSWP) is a compiler optimization that leverages pipelined parallelism [15][12], illustrated in Figure 1b. The dependencies are communicated between threads using asynchronous channels, which can be implemented as a shared queue in memory or in hardware [13]. Unlike DOACROSS, communication latencies and stalls will only affect consuming threads, allowing the producing threads to work ahead. DSWP is capable of a significant performance increase: in the SPEC CINT2000 benchmark suite, DSWP yielded a geometric mean speedup of 5.54 with a geometric mean of 17 threads [1].

In Section 2 we will show how to parallelize a wide class of programs. In Section 4 we will show how to transform SL proofs of sequential programs into CSL proofs of DSWP-parallelized programs.

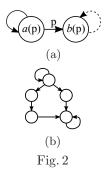
Concurrent Separation Logic for Pipelined Parallelization

while c(p) ( while c(p) ( b(p); p:= a(p)) Fig. 3: Running example  $\begin{pmatrix} produce d p;\\ while c(p) (\\ p:= a(p);\\ produce d p \end{pmatrix}$   $\begin{pmatrix} consume d p';\\ while c(p') (\\ b(p');\\ consume d p' \end{pmatrix}$ 

Fig. 5: Parallelized while-program

# 2 Parallelizing a Program

To illustrate our operational semantics and CSL, we consider the class of programs in Figure 3, where  $a(\mathbf{p})$  and  $b(\mathbf{p})$  represent blocks of instructions that use at least variable  $\mathbf{p}$ . We assume operation  $a(\mathbf{p})$  does not depend on  $b(\mathbf{p})$ ,  $b(\mathbf{p})$  depends only on  $a(\mathbf{p})$  exactly through variable  $\mathbf{p}$ , and  $b(\mathbf{p})$  may or may not depend on itself through variables other than  $\mathbf{p}$ ; illustrated in Figure 2a. Figure 4 is an example of such a program. The dependencies in Figure 2a also generalize over more complicated dependencies such as in Figure 2b. In practice, tasks  $a(\mathbf{p})$  and  $b(\mathbf{p})$  are significant computations.



This program is *not* a candidate for DOALL optimization because of the loopcarried dependencies from  $a(\mathbf{p})$  to  $a(\mathbf{p})$  and possibly from  $b(\mathbf{p})$  to  $b(\mathbf{p})$ . However, because the dependency between  $a(\mathbf{p})$  and  $b(\mathbf{p})$  is in one direction, we can apply DSWP to generating the program in Figure 5.

This parallelized program, where we have two processes communicating using instructions produce and consume, computes the same values as Figure 3. To send the value of expression e through channel d (pushing the value onto the back of the channel's queue), we write produce d e. To receive a value (from the front of the channel's queue) into variable x, we write consume d x.

## 3 CSL with Asynchronous Channels

Our logic is an extension of SL with channel endpoints and the heap as resources. We treat channels as a way to transmit both values and resources. While a lowlevel view of a program may simply see integers being sent through a channel, in our logic those integers may have further meaning. For example, they can be channel identifiers or pointers. When transmitting a pointer, we can bundle the

knowledge that it is a pointer (with permission to dereference it) as a resource, and send the resource along with the pointer value.

To control how the channels are used, we assign resource invariants to each channel to act as a protocol, to which producing and consuming processes must adhere. A resource invariant is a predicate that must always hold on the state of the channel. Resource invariants were introduced to CSL by O'Hearn and have been used to control how critical sections and locks are used [9][6]. Producers use the resource invariant to determine which resources they must give up when sending a value. Consumers use the resource invariant to determine which resources they gain by receiving a value. For example, a resource invariant could state that each value in the channel points to an integer: producers must show that each value sent is such a pointer and give up the resource to dereference it, and consumers use the resource invariant to show that each received value is a valid pointer that can be dereferenced.

#### 3.1 Channel endpoint histories

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A main property of CSL is that we reason about the correctness of a process independently of all other processes. When a process sends a value to another process through a channel, neither knows what the other has or will do to the value beyond what the resource invariant states. This is enough for memory safety; access to a shared pointer can be transferred between processes to prevent race conditions. However, resource invariants cannot show that values transmitted by a producing process are correctly summed by a consuming process. We also cannot use them to ensure that every pointer sent through a channel is eventually deallocated. Local reasoning in CSL prevents us from reasoning about these behaviors from the perspective of just one process. To overcome this limitation, we delay such reasoning, by recording a *history* of the values transmitted through each endpoint, until the processes synchronize.

**Histories in point-to-point communication.** Consider two processes: a producer and consumer. The producer sends 1 followed by 2, so its history is [2, 1]. The consumer receives two values and stores them into variable x, then y. Because the consumer cannot know what the producer sent, its history is simply [y, x]. When the two processes join, we know that [2, 1] was sent and that [y, x] was received, so [y, x] = [2, 1], or y = 2 and x = 1.

**Histories with multiple producers and consumers.** We allow a channel endpoint to be split among multiple producers or consumers. Each piece of an endpoint records its own *local* history, and when all the pieces of an endpoint are joined, the history is *global*. Recording histories through a piece of an endpoint is trickier than recording the history in the full endpoint because the order in which the processes send/receive from the channel is nondeterministic. For this reason, we record *sets* of possible histories through each endpoint.

$A ::= d_{\pi} H!$	Share $\pi$ of the produce endpoint of channel d, with histories H
$d_{\pi}H?$	Share $\pi$ of the consume endpoint of channel $d$ , with histories $H$
$ A[\mathbf{p}: d \neq v]$	A holds after appending $v$ to $d$ 's local produce histories
$ A[c: d \neq v]$	A holds after appending $v$ to $d$ 's local consume histories
PHist $d H$	The local produce histories of channel $d$ are $H$
CHist $d H$	The local consume histories of channel $d$ are $H$
$e \Downarrow v$	The expression evaluates to value $v$
$  e_1 \mapsto e_2   A_1$	$*A_2 \mid A_1 \twoheadrightarrow A_2 \mid A_1 \Longrightarrow A_2 \mid e_1 = e_2 \mid e_2 \mid B$

#### Fig. 6: Predicates

Consider the case of multiple processes producing through the same channel. Each producer records the sequence of the values it sends, but not what other producers send. When two of the processes join, we do not know the order of one history with respect to the other. Thus the combined endpoint records all possible orderings by interleaving the two histories; the actual order in which the values were sent must be within this set. When a new value is subsequently produced through the endpoint, it is appended to each history in the set.

When two sets of histories join, we compute the new set of histories by interleaving every pair of histories from the two sets. We call this operation a *merging* of the histories. Every history in a set of histories is a permutation of all other histories in the set; merging preserves this behavior. For multiple consumers, we record histories in the same way.

Example 1 (Multiple consumers). Assume we have one producing process and two consuming processes, each with an initial set of histories equal to  $\{nil\}$  (none have sent or received any values). The producer sends 1, 2, 3, then 4. Consumer 1 receives two values, w then x; consumer 2 receives one value, y; then they join and one more value, z, is consumed. The resulting sets of histories are:

Producer	Consumer 1	Consumer 2	After C1 & C2 join, then consume $z$
$\{[4, 3, 2, 1]\}$	$\{[x,w]\}$	$\{[y]\}$	$z::(\{[x,w]\} \land \{[y]\}) =$
			$z{::}\{[x,w,y],[x,y,w],[y,x,w]\} =$
			$\{[z, x, w, y], [z, x, y, w], [z, y, x, w]\}$

The merged ( $\mathbb{M}$ ) consume histories cannot exactly reconstruct the order in which the two consumers received values with respect to each other. They can show, however, that z = 4 and z > x > w.

## 3.2 Predicate logic

Figure 6 lists some predicates used in our logic. Metavariable A is a predicate that ranges over formulae, e is an expression, H is a set of histories (each a list of values), and d is a channel name.  $\pi$  is a fractional share of a resource that ranges over [0, 1], where  $\pi > 0$  grants permission for [shared] use of the resource

and  $\pi = 0$  does not. A value is either an integer or list of values. The predicates in the last line are conventional: separating conjunction, separating implication, implication, expression equality, no share of any resources, and a pure logical formula. The logic has universal and existential quantification ranging over values. We use the forcing relation  $r; s \models A$  to state that predicate A holds under environment s and exactly resources r (resources are defined in Section 5.1). Predicate  $A_1$  entails  $A_2$  if  $\forall r, s. r; s \models A_1 \implies r; s \models A_2$ , written  $A_1 \vdash A_2$ .

Predicates PHist/CHist hold for any resource if the produce/consume history is exactly H. They are used as side conditions for some of the Hoare rules.

Channel endpoints interact with the separating conjunction as follows:

$$\begin{aligned} d_{\pi_1} H_1! * d_{\pi_2} H_2! &\iff d_{\pi_1 + \pi_2} (H_1 \land \!\!\!\land H_2)! \\ d_{\pi_1} H_1? * d_{\pi_2} H_2? &\iff d_{\pi_1 + \pi_2} (H_1 \land \!\!\!\land H_2)? \end{aligned}$$

Example 2. Assume that Example 1 uses channel d and the two consumers have permissions  $\pi_1$  and  $\pi_2$ . Just before the consumers join, they have resources  $d_{\pi_1}\{[x,w]\}$ ? and  $d_{\pi_2}\{[y]\}$ ? respectively. After joining, their resources are:

$$d_{\pi_1}\{[x,w]\}? * d_{\pi_2}\{[y]\}? \vdash d_{\pi_1+\pi_2}(\{[x,w]\} \land \{[y]\})? \\ \vdash d_{\pi_1+\pi_2}\{[x,w,y], [x,y,w], [y,x,w]\}?$$

And after consuming into variable z, their resources are:

$$d_{\pi_1+\pi_2}(z::\{[x,w,y],[x,y,w],[y,x,w]\})? \\ \vdash d_{\pi_1+\pi_2}\{[z,x,w,y],[z,x,y,w],[z,y,x,w]\}?$$

#### 3.3 Resource invariants

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We use resource invariants to verify that values and resources are transmitted through each channel according to protocol. The state of a channel is composed of the resources r stored in the channel, the list of values  $l_q$  queued in the channel, and the list of previously consumed values  $l_c$  (not a *set* of histories). A resource invariant R holds on the state  $(r, l_q, l_c)$  of a channel only if r;  $\models$  $R(l_q, l_c)$ . Concatenating the queue  $l_q$  and consume values  $l_c$  of a channel together, written  $l_q@l_c$ , yields the list of produced values for the channel. Channel resource invariants must satisfy the predicate  $\vdash R \text{ R-okay}$ , specified as follows:

emp 
$$\vdash R(\text{nil}, \text{nil})$$
  
 $\forall l_q, l_c. R(l_q, l_c) \text{ is closed and precise}$   
 $\frac{\forall l_c. R(\text{nil}, l_c) \vdash \text{emp}}{\vdash R \text{ R-okay}}$  Resource-Okay

The first premise states that the resource invariant must be satisfied and own no resources for a channel that has not yet been used. The second ensures that resources can be transferred between process environments and that the resource invariant is sufficient to determine exactly what resources are transferred to and  $\iota ::= \iota_1; \iota_2 | x := e | x := [e] | [x] := e | \text{ while } e \iota | \text{ assert } A | [\Gamma_1; A_1] \iota_1 \parallel [\Gamma_2; A_2] \iota_2 | \text{ produce } d e | \text{ consume } d x | \text{ skip}$ 

Instruction sequencing, local variable assignment, fetch from heap, store into heap, repeat  $\iota$  until e is false, assert that predicate A holds, run two blocks of instructions in parallel, produce a value, consume a value into a local variable, no-op.

Fig. 7: Instructions

from the channel. Finally, the third premise attaches resources only to values in the queue and not the consume history to ensure that all resources can eventually be extracted from the channel by consuming values.

*Example 3.* A resource invariant that specifies the first value produced/consumed is 0 and that the values transmitted are strictly increasing:

$$\begin{split} R &\triangleq \lambda l_q.\lambda l_c. \text{ match } l_q, l_c \text{ with} \\ &| \text{ nil, nil} \Rightarrow \text{emp} \\ &| \text{ nil, v::nil} \Rightarrow v = 0 \land \text{emp} \\ &| \text{ nil, } v_1 :: v_2 :: l_c \Rightarrow v_1 > v_2 \land R(\text{nil, } v_2 :: l_c) \\ &| l_q @v::nil, l_c \Rightarrow R(l_q, v:: l_c) \end{split}$$

*Example 4.* A resource invariant for the parallelization of Figure 4 in Figure 5. To pass permission to dereference p.val through the channel:

$$\begin{split} R &\triangleq \lambda l_q.\lambda l_c. \text{ match } l_q, l_c \text{ with} \\ &\mid \text{nil}, \_ \Rightarrow \text{emp} \\ &\mid v{::}l'_q, \_ \Rightarrow R(l'_q, l_c) * v.\texttt{val} \mapsto - \end{split}$$

### 3.4 Instructions

In Figure 7, x is a program variable,  $\iota$  is an instruction, A is a predicate,  $\Gamma$  is a set of free variables, and d is the name of a channel. Instruction  $[\Gamma_1; A_1] \iota_1 \parallel [\Gamma_2; A_2] \iota_2$  uses  $\Gamma$  and A to specify how variables and resources are split between processes  $\iota_1$  and  $\iota_2$ . We use **assert** to prove the partial correctness of programs.

### 3.5 Hoare logic

A Hoare triple describes the precondition and postcondition of executing a command. If the precondition is met and the command terminates, then the postcondition establishes the new state of the program. We give the Hoare triple rules for our logic in Figure 8. FV(X) denotes the set of free variables in X, where X ranges over instructions and predicates. The Hoare triple  $\overline{R}$ ;  $\Gamma \vdash_i \{A\} \ \iota \ \{B\}$ is composed of an instruction  $\iota$ , precondition A, postcondition B, environment

$$\begin{split} l \in_{\pi} H &\triangleq \begin{cases} l \in H & \text{if } \pi = 1 \\ \exists H'. l \in H \land H' & \text{if } \pi \neq 1 \end{cases} \\ & B \vdash \text{PHist } d \{\text{nil}\} & A \vdash \text{PHist } d e::H \\ & \forall l_q, l_c. l_q @l_c \in_{\pi} H \Longrightarrow B * \tilde{R}[d](l_q, l_c) \vdash \tilde{R}[d](e::l_q, l_c) \\ & \overline{R}; \Gamma \vdash_i \{d_{\pi} H! * (d_{\pi} e::H! \twoheadrightarrow B * A)\} \text{ produce } d \in \{A\} \end{cases} \text{ H-Produce} \\ & x \in \Gamma \quad \forall v. B(v) \vdash \text{CHist } d \{\text{nil}\} \quad A \vdash \text{CHist } d x::H \\ & \forall l_q, v, l_c. l_c \in_{\pi} H \Longrightarrow \\ & \overline{R}[d](l_q @v::ni, l_c) \vdash B(v) * \overline{R}[d](l_q, v::l_c) \\ \hline \overline{R}; \Gamma \vdash_i \{d_{\pi} H? * (\forall v. (d_{\pi} H? * B(v))]c: d + = v] \twoheadrightarrow A[v/x]) \} \\ & \text{consume } d x \\ & \frac{\overline{R}; \Gamma_1 \vdash_i \{A_1\} v_1 \{B_1\} \quad FV(A_1) \subseteq \Gamma_1 \quad \Gamma_1 \# \Gamma_2 \\ \hline \overline{R}; \Gamma \vdash_i \{A_1 A * A_2\} [\Gamma_1; A_1] v_1 \parallel [\Gamma_2; A_2] v_2 \{B_1 * B_2\} \\ & \text{H-Parallel} \\ \hline \hline \overline{R}; \Gamma \vdash_i \{A_1 * A_2\} [\Gamma_1; A_1] v_1 \parallel [\Gamma_2; A_2] v_2 \{B_1 * B_2\} \\ & \text{H-Fetch} \\ \hline \hline \overline{R}; \Gamma \vdash_i \{A_1 \approx e \Rightarrow v * (e \mapsto v \ast A[v/x])\} x := [e] \{A\} \\ & \text{H-Fetch} \\ \hline \hline \overline{R}; \Gamma \vdash_i \{A_1 \approx e_i \mapsto e_i \leftrightarrow e_i \land A[v]\} \\ \hline \hline \overline{R}; \Gamma \vdash_i \{A_1 \approx e_i \mid A \mid B \\ & \overline{R}; \Gamma \vdash_i \{A_1 \circ A \mid B \} \\ \hline FV(t) \cap FV(C) = \emptyset \\ & \forall d \in FV(t) \cap C \vdash PHist d \{nil\} \land CHist d \{nil\} \\ \hline \overline{R}; \Gamma \vdash_i \{A\} v \{B\} \quad FV(i) \cap FV(C) = \emptyset \\ & \forall d \in FV(i) \cap C \vdash PHist d \{nil\} \land CHist d \{nil\} \\ \hline \overline{R}; \Gamma \vdash_i \{A\} v \{B\} \\ \hline \overline{R}; \Gamma \vdash_i \{A\} v \{B\} \\ \hline FV_i \leftarrow B \times C \end{cases} \\ \hline \hline \frac{\overline{R}; \Gamma \vdash_i \{A\} v \{B\} \\ \hline \overline{R}; \Gamma \vdash_i \{A\} v \{B\} \\ \hline FV(i) = e i \{A \land \neg e\} \\ \hline FV(i) = e i \{A \land \neg e\} \\ \hline FV(i) = e i \{A \land \neg e\} \\ \hline FV(i) = e i \{A \land \neg e\} \\ \hline FV(i) = e i \{A \land \neg e\} \\ \hline FV(i) = e i \{A \land \neg e\} \\ \hline FV(i) = e i \{A \land \neg e\} \\ \hline FV(i) = e i \{A \land \neg e\} \\ \hline FV(i) = e i \{A \land \neg e\} \\ \hline FV(i) = e i \{A \land \neg e\} \\ \hline FV(i) = e i \{A \land \neg e\} \\ \hline FV(i) = e i \{A \land \neg e\} \\ \hline FV(i) = e i \{A \land \neg e\} \\ \hline FV(i) = e i \{A \land \neg e\} \\ \hline FV(i) = e i \{A \land \neg e\} \\ \hline FV(i) = e i \{A \land \neg e\}$$

Fig. 8: Inference rules of the Hoare logic

domain  $\Gamma$ , and a channel-indexed list of resource invariants  $\overline{R}$ . We write  $\Gamma_1 \# \Gamma_2$ if the two domains are disjoint. For any element X in our formal system, we write  $\overline{X}$  to denote a list of such elements and  $\overline{X}[i]$  to access the  $i^{\text{th}}$  element.

*H-Produce.* Consider a program that produces pointers to nodes in a linked list with the intention that the consumer only accesses the val member of each node, such as in Figure 5. To execute produce d p and express that  $p.val \mapsto -$  is transferred to the channel (to eventually be transferred to a consumer), that the produce histories are appended with p, and that the resource  $p.next \mapsto -$  is retained, we could use the Hoare triple and resource invariant:

$$\begin{split} \bar{R}; \Gamma \vdash_{\mathbf{i}} \{ d_1 H! * \mathrm{p.val} \mapsto - * \mathrm{p.next} \mapsto - \} \text{ produce } d \neq \{ d_1 \mathrm{p}::H! * \mathrm{p.next} \mapsto - \} \\ \bar{R}[d] \triangleq \lambda l_q. \lambda l_c. \text{ match } l_q, l_c \text{ with} \\ | \text{ nil}, \_ \Rightarrow \text{ emp} \\ | v::l'_q, \_ \Rightarrow R(l'_q, l_c) * v. \mathtt{val} \mapsto - \end{split}$$

To prove this triple, we apply rules H-Produce and H-Consequence and prove these side conditions:

$$\forall l_q, l_c. \ l_q @l_c \in H \implies (p.val \mapsto - * R(l_q, l_c) \vdash R(p::l_q, l_c))$$
(1)

$$p.val \mapsto - \vdash PHist \ d \ \{nil\}$$
(2)

$$d_1 p:: H! * p.next \mapsto - \vdash PHist \ d \ p:: H$$
 (3)

$$\begin{pmatrix} d_1 H! * p.\mathsf{val} \mapsto - \\ * p.\mathsf{next} \mapsto - \end{pmatrix} \vdash \begin{pmatrix} d_1 H! * (d_1 p::H! - * (p.\mathsf{val} \mapsto - ) \\ * d_1 p::H! * p.\mathsf{next} \mapsto - ) \end{pmatrix}$$
(4)

These obligations are easy to prove for this example. (The antecedent in obligation 1 can be ignored because it is not needed to prove the consequent).

Rule H-Produce requires some permission  $(d_{\pi}H!)$  to access the produce endpoint and implies that the post state will have histories H appended with the value sent. The first judgement in H-Produce,  $B \vdash$  PHist d {nil}, prevents the resources B that are transferred to the channel from specifying histories for the same channel. Judgement  $A \vdash$  PHist d e:: H prevents the postcondition from specifying histories in addition to e::H. These side conditions involving PHist and CHist are necessary to prove soundness using our current model of histories. They do not prevent channels from sending shares of themselves (with histories {nil}) or shares and histories of other channels.

The third judgement requires that, for any state of the channel (the queue  $l_q$  and consumed values  $l_c$ ) such that the resource invariant holds, the invariant remains satisfied after pushing e onto the back of the queue and adding resources B to the channel. Its antecedent,  $l_q@l_c \in_{\pi} H$ , restricts the set of channel states to those that support the local histories we have observed.

When  $\pi = 1$ ,  $l_q@l_c \in_{\pi} H$  simplifies to  $l_q@l_c \in H$  (*H* contains all possible orderings of produced values), and when  $\pi < 1$ , it implies that every value in *H* is present in the list of produced values  $l_q@l_c$ . This constraint, although weak, still has uses. For example, it allows producing a 0 to a channel with the resource invariant "all values must be 1 until a 0 is produced, at which point only 0's can be produced" if all we know is that a 0 appears in the local produce histories.

*H-Consume.* Consider the consumer process from the previous example program, which consumes values that are pointers to nodes in a linked list, only to dereference the val member of each node. To execute consume d p', express that  $p'.val \rightarrow -$  is received from the channel, and that the consume histories are appended with p', we could use the Hoare triple:

$$\overline{R}; \Gamma, x \vdash_{i} \{d_1H?\}$$
 consume  $d$  p'  $\{d_1p'::H?*p'.val \mapsto -\}$ 

To prove this triple, we apply rules H-Consume and H-Consequence and prove:

$$\forall l_q, v, l_c. \ l_c \in_1 H \implies \left( R(l_q @v::nil, l_c) \vdash v.\mathsf{val} \mapsto - * R(l_q, v::l_c) \right) \tag{5}$$
$$v.\mathsf{val} \mapsto - \vdash \text{CHist } d \text{ {nil}} \tag{6}$$

$$d_1 \mathbf{p}' :: H^2 * \mathbf{p}' \text{ val} \mapsto - \vdash \text{CHist } d \mathbf{p}' :: H \tag{7}$$

$$(I) = (II2 + ($$

$$d_1H? \vdash \begin{pmatrix} d_1H? * (\forall v. (d_1H? * v.val \mapsto -)[\mathsf{c}: d+=v] \\ -* (d_1\mathsf{p}'::H? * \mathsf{p}'.val \mapsto -)[v/\mathsf{p}'] \end{pmatrix}$$
(8)

These particular obligations are also easy to prove. Obligation 8, although convoluted, can be deduced easily:

$$\begin{split} d_1H? \vdash \begin{pmatrix} d_1H?*\left(\forall v.\ (d_1H?*v.\mathsf{val}\mapsto -)[\mathsf{c}:\ d+=v] \\ -*\ (d_1\mathsf{p}'::H?*\mathsf{p}'.\mathsf{val}\mapsto -)[v/\mathsf{p}'] \right) \end{pmatrix} \\ emp \vdash \begin{pmatrix} \forall v.\ (d_1H?*v.\mathsf{val}\mapsto -)[\mathsf{c}:\ d+=v] \\ -*\ (d_1\mathsf{p}'::H?*\mathsf{p}'.\mathsf{val}\mapsto -)[v/\mathsf{p}'] \end{pmatrix} \end{pmatrix} \\ (d_1H?*v.\mathsf{val}\mapsto -)[\mathsf{c}:\ d+=v] \vdash (d_1\mathsf{p}'::H?*\mathsf{p}'.\mathsf{val}\mapsto -)[v/\mathsf{p}'] \\ d_1v::H?*v.\mathsf{val}\mapsto -\vdash d_1v::H?*v.\mathsf{val}\mapsto - \end{split}$$

Rule H-Consume requires permission  $(d_{\pi}H^2)$  to access the consume endpoint. The fourth judgement in H-Consume requires that, for all states of the channel (the queue  $l_q@v::nil$  and consumed values  $l_c$ ) such that its resource invariant holds, the invariant remains satisfied after popping v from the front of the queue, recording it in the list of consumed values, and removing the resources B(v) tied to the value. (B is a function from values to predicates). The antecedant,  $l_c \in_{\pi} H$ , restricts the consumed values to those that are supported by the local consume histories. Resources B(v) are transferred to the consuming process. Finally, the local consume histories are appended with the consumed value.

# 4 Parallelized Program with Proof

Consider proofs of correctness for programs such as Figure 3 (and particularly Figure 4) that follow the schema in Figure 9. We give an example instance of such

a proof in Figure 10 for the program in Figure 4. The example proof ensures that the shape and order of the linked list is preserved, and holds for the properties:

$$\bar{R}; \Gamma \vdash_{i} \{C(h, \mathbf{p}) * D(h) \land c(\mathbf{p}) \land \mathbf{p} \Downarrow v\}$$

$$\mathbf{p} := a(\mathbf{p})$$

$$\{F(\mathbf{p}) * D(h) * C(v::h, \mathbf{p}) \land c(v)\}$$

$$\bar{R}; \Gamma \vdash_{i} \{C(h, \mathbf{p}) * F(\mathbf{p}) * D(h) \land c(\mathbf{p})\} b(\mathbf{p}) \{C(h, \mathbf{p}) * D(\mathbf{p}::h) \land c(\mathbf{p})\}$$
(10)

Furthermore, if the following properties hold, then we can construct a proof for programs characterized by Figure 3 and optimized by DSWP:

$$\bar{R}; \Gamma \vdash_{i} \{ C(h, \mathbf{p}) \land c(\mathbf{p}) \land \mathbf{p} \Downarrow v \} \mathbf{p} := a(\mathbf{p}) \{ F(\mathbf{p}) * C(v::h, \mathbf{p}) \land c(v6) \}$$
(11)

$$\bar{R}; \Gamma \vdash_{i} \{F(\mathbf{p}) * D(h) \land c(\mathbf{p})\} \ b(\mathbf{p}) \ \{D(\mathbf{p}::h) \land c(\mathbf{p})\}$$
(12)

$$FV(b(p)) \cap MV(p:=a(p)) = p$$
 (13)

$$FV(c(p)) \cap MV(p := a(p)) = p$$
 (14)

$$FV(c(p)) \cap MV(b(p)) = \emptyset$$
 (15)

The program in Figure 4, using the definitions in Figure 10, satisfies properties 9-15 and can be transformed into a parallelized proof. Such properties are fairly typical for programs in the general schema of Figure 3. Our technique applies to programs with a simple dependency structure,  $\bigcirc$ , which is a generalization of more complicated structures:

instance in Figure 5.

**Theorem 1.** Given any program instance of Figure 3 with a (sequential) Separation Logic proof given by (9) and (10), and satisfying (11)-(15), there is a Concurrent Separation Logic proof of the correctness of the parallelized program

## 4.1 Proof of Theorem 1

The proof in Figure 9 has three separated predicate functions, C, D, and F to model the resources attached to the dependencies flowing from  $a(\mathbf{p})$  to  $a(\mathbf{p})$ ,  $b(\mathbf{p})$  to  $b(\mathbf{p})$ , and  $a(\mathbf{p})$  to  $b(\mathbf{p})$ , respectively. The logical variable h is used to reason about past values of  $\mathbf{p}$ . The association of C to  $a(\mathbf{p})$  is supported by property 11,



and D to  $b(\mathbf{p})$  by property 12. The resources F are shown to be generated by  $a(\mathbf{p})$  and transferred to  $b(\mathbf{p})$  by properties 11 and 12, following the dependence of  $b(\mathbf{p})$  on  $a(\mathbf{p})$  through variable  $\mathbf{p}$ . Property 13 restricts the dependency between  $a(\mathbf{p})$  and  $b(\mathbf{p})$  to just variable  $\mathbf{p}$ , and properties 14 and 15 restrict control flow dependencies to just  $\mathbf{p}$ . The notation  $FV(\iota)$  is the set of free variables in  $\iota$  and  $MV(\iota)$  is the set of modified variables.

**Constructing the parallelized proof.** Applying the DSWP optimization to this program results in the program in Figure 5 (for a fresh channel  $d \notin \overline{R}$ ). To construct a proof for the parallelized program, we reuse elements of the original proof. First, we introduce a predicate to help prove that the consumer will receive all values sent.

$$T \triangleq \lambda h. \text{ match } h \text{ with}$$
$$| \text{ nil} \Rightarrow \text{true}$$
$$| v::h' \Rightarrow c(v) \land T(h')$$

Then, we create a new variable context ( $\Gamma' \triangleq \Gamma, \mathbf{p}^{\prime}, h'$ ) and new resource invariants  $\overline{R}'$  to allow resources  $F(\mathbf{p})$  to be produced and consumed through channel d. The new resource invariant satisfies  $\forall d'. d \neq d' \implies \overline{R}'[d'] = \overline{R}[d']$  and:

$$R'[d] \triangleq \lambda l_q, \ \lambda l_c. \text{ match } l_q, l_c \text{ with}$$
$$| \text{ nil}, \_ \Rightarrow \text{ emp}$$
$$| l'_a @v::nil, \_ \Rightarrow F(v) * \overline{R}'[d](l'_a, v::l_c)$$

We start the parallelized program with the same precondition as the original, but add produce and consume endpoints  $d_1{\text{nil}}!$  and  $d_1{\text{nil}}?$  to enable access to the channels. Using rules H-Frame and H-Consequence on property 11, we get:

$$\bar{R}'; \Gamma' \vdash_{i} \{ d_{1}\{\mathbf{p}::h\}! * C(h, \mathbf{p}) \land T(h) \land c(\mathbf{p}) \land \mathbf{p} \Downarrow v \}$$
$$\mathbf{p}:= a(\mathbf{p})$$
$$\{ d_{1}\{\mathbf{p}::h\}! * F(\mathbf{p}) * C(v::h, \mathbf{p}) \land T(h) \land c(v) \}$$

Which, for brevity, we rewrite as:

$$\bar{R}'; \Gamma' \vdash_{i} \{A(h, \mathbf{p}) \land c(\mathbf{p}) \land \mathbf{p} \Downarrow v\} \mathbf{p} := a(\mathbf{p}) \{F(\mathbf{p}) \ast A'(v::h, \mathbf{p})\}$$

$$\begin{split} \bar{R}'; \Gamma' \vdash_{\iota} & \{C(\text{nil}, p) * F(p) * D(\text{nil}) * d_{1}\{\text{nil}\}! * d_{1}\{\text{nil}\}? \land T(\text{nil})\} \\ & \{F(p) * A'(\text{nil}, p) * B'(\text{nil})\} \\ & \{F(p) * A'(\text{nil}, p)\} \\ & \text{produce } d \text{ p}; \\ & \{\exists h. \ A(h, p)\} \\ & \text{while } c(p) ( \\ & \{\exists h. \ A(h, p) \land c(p)\} \\ & \{A(h, p) \land c(p) \land p \Downarrow v\} \\ & p:= a(p); \\ & \{F(p) * A'(v::h, p)\} \\ & produce \ d \text{ p} \\ & \{\exists h. \ A(h, p)\} \\ & \\ & \{\exists h. \ A(h, p)\} \\ & \\ & \{\exists h. \ A(h, p)\} \\ & \\ & \{\exists h. \ A(h, p) \land \neg c(p)\} \\ & \{F(p') * \exists h'. \ B(h', p') \land c(p')\} \\ & \{F(p') * \exists h'. \ B(h', p') \land c(p')\} \\ & \{F(p') * \exists h'. \ B(h', p') \land c(p')\} \\ & \{F(p') * \exists h'. \ B(h', p') \land c(p')\} \\ & \{F(p') * \exists h'. \ B(h', p') \land c(p')\} \\ & \{A(h, p) * F(p') * B(h', p') \land \neg c(p')\} \\ & \{F(p') * \exists h'. \ B(h', p') \land \neg c(p')\} \\ & \{C(h, p) * F(p) * D(h) * d_{1}\{p::h\}! * d_{1}\{p::h\}? \land \neg c(p)\} \\ & \text{assert } C(h, p) * F(p) * D(h) \land \neg c(p) \end{split}$$

Fig. 11: Parallelized while-program with proof

where:

$$A(h, \mathbf{p}) \triangleq d_1\{\mathbf{p}::h\}! * C(h, \mathbf{p}) \wedge T(h)$$
$$A'(h, \mathbf{p}) \triangleq d_1\{h\}! * C(h, \mathbf{p}) \wedge T(h)$$

We do the same for property 12:

$$\begin{split} \bar{R}'; \Gamma' \vdash_{\mathbf{i}} & \{ d_{\pi} \{ \mathbf{p} :: h \}? * F(\mathbf{p}) * D(h) \wedge c(\mathbf{p}) \} \\ & b(\mathbf{p}) \\ & \{ d_{\pi} \{ \mathbf{p} :: h \}? * D(\mathbf{p} :: h) \wedge c(\mathbf{p}) \} \\ \bar{R}'; \Gamma' \vdash_{\mathbf{i}} & \{ F(\mathbf{p}) * B(h, \mathbf{p}) \wedge c(\mathbf{p}) \} \\ & b(\mathbf{p}) \\ & \{ B'(\mathbf{p} :: h) \wedge c(\mathbf{p}) \} \end{split}$$

where:

$$B(h, \mathbf{p}) \triangleq d_1\{\mathbf{p}::h\}? * D(h)$$
$$B'(h) \triangleq d_1\{h\}? * D(h)$$

Next, we prove the hoare triples for producing values, and rewrite the triple using A and A' for brevity:

$$\begin{split} \bar{R}'; \Gamma' \vdash_{i} & \{F(\mathbf{p}) * d_{1}\{v::h\}! * C(v::h,\mathbf{p}) \wedge T(h)\} \\ & \text{produce } d \text{ p} \\ & \{F(\mathbf{p}) * d_{1}\{\mathbf{p}::v::h\}! * C(v::h,\mathbf{p}) \wedge T(h)\} \\ \bar{R}'; \Gamma' \vdash_{i} & \{F(\mathbf{p}) * A'(v::h,\mathbf{p}))\} \text{ produce } d \text{ p } \{\exists h. \ A(h,\mathbf{p})\} \end{split}$$

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We do the same for consuming values:

$$\begin{split} \bar{R}'; \Gamma' &\vdash_{i} \{ d_{1}\{\mathbf{p}'::h'\}? * D(\mathbf{p}'::h') \} \\ & \text{consume } d \mathbf{p}' \\ \{ F(\mathbf{p}') * \exists v. \ d_{1}\{\mathbf{p}'::v::h'\}? * D(v::h') \} \\ \bar{R}'; \Gamma' &\vdash_{i} \{ B'(\mathbf{p}'::h') \} \text{ consume } d \mathbf{p}' \{ F(\mathbf{p}') * \exists h'. \ B(h', \mathbf{p}') \} \end{split}$$

The last step is to prove:

$$A(h, \mathbf{p}) * F(\mathbf{p'}) * B(h', \mathbf{p'}) \land \neg c(\mathbf{p'})$$
$$\vdash C(h, \mathbf{p}) * F(\mathbf{p}) * D(h) * d_1\{\mathbf{p}::h\}! * d_1\{\mathbf{p}::h\}? \land \neg c(\mathbf{p})$$

Proof.

$$A(h, \mathbf{p}) * F(\mathbf{p'}) * B(h', \mathbf{p'}) \land \neg c(\mathbf{p'})$$
$$\vdash (d_1\{\mathbf{p}::h\}! * C(h, \mathbf{p}) \land T(h)) * F(\mathbf{p'}) * (d_1\{\mathbf{p'}::h'\}? * D(h')) \land \neg c(\mathbf{p'})$$

At this point, we know that since all values consumed were produced at some point,  $\exists l. p::h = l@p'::h'$ . (This is encoded in our resources: for all  $l_q$ , the intersection of the global produce histories and global consume histories, appended with  $l_q$ , cannot be empty). If l = v::l', then T(l'@p'::h'), which implies c(p'). This is a contradiction, so l = nil and p::h = p'::h'. Thus p = p' and h = h'

$$(d_1\{\mathbf{p}::h\}! * C(h, \mathbf{p}) \land T(h)) * F(\mathbf{p}) * (d_1\{\mathbf{p}::h\}? * D(h)) \land \neg c(\mathbf{p}) \vdash C(h, \mathbf{p}) * F(\mathbf{p}) * D(h) * d_1\{\mathbf{p}::h\}! * d_1\{\mathbf{p}::h\}? \land \neg c(\mathbf{p})$$

We add the **assert** instruction to the end of the program to ensure partial correctness, encoded as a safety property. If the asserted condition cannot be proven, then the instruction will get stuck and the program will not be safe.

Figure 11 is the proof for the parallelized program in Figure 5, such that the preconditions and postconditions (modulo the addition of channel endpoints) are preserved.

# 5 Model & Operational Semantics

#### 5.1 The Separation Algebra of resources

A standard technique [3] for constructing a SL is to first construct a Separation Algebra (SA) on the resources. Our CSL is based on the SA of *worlds*, which are composed of three kinds of resources: the heap, produce endpoints, and consume endpoints. Although the heap is not necessary to demonstrate a CSL for channels, we include it to prove the correctness of parallelized pointer-programs, where channels are used to synchronize access to shared memory and prevent race conditions. We have formalized<sup>1</sup> our SA following Dockins et al. [2].

<sup>&</sup>lt;sup>1</sup> A Coq formalization of our SA is available at http://www.cs.princeton.edu/ ~cbell/cslchannels/

$$\begin{split} \pi \in \operatorname{Share} &\triangleq [0,1] & u \in \operatorname{Location} \\ d \in \operatorname{ChannelName} & H \in \operatorname{HistorySet} \\ & \operatorname{Endpoint} \triangleq \{ (\pi, H) : \operatorname{Share} \times \operatorname{HistorySet} \mid \pi = 0 \implies H = \{\operatorname{nil}\} \} \\ r : \{ \operatorname{m} : \operatorname{Location} \to \operatorname{option} \operatorname{value}, \\ p : \operatorname{ChannelName} \to \operatorname{option} \operatorname{Endpoint}, \\ c : \operatorname{ChannelName} \to \operatorname{option} \operatorname{Endpoint} \} \\ & \frac{\forall x. \ f_1(x) \oplus f_2(x) = f_3(x)}{f_1 \oplus_f f_2 = f_3} \quad \operatorname{Join-Function} \\ \\ \frac{\pi_1 \oplus_s \pi_2 = \pi_3}{H_1 \wedge H_2 = H_3} \\ \overline{(\pi_1, H_1) \oplus_e(\pi_2, H_2)} = (\pi_3, H_3) \quad \operatorname{Join-Endpoint} \quad \frac{ \begin{array}{c} r_1.m \oplus_f r_2.m = r_3.m \\ r_1.p \oplus_f r_2.p = r_3.p \\ r_1.c \oplus_f r_2.c = r_3.c \\ r_1 \oplus_w r_2 = r_3 \end{array} \quad \operatorname{Join-World} \end{split}$$

## Fig. 12: Channel Resources

A SA is a tuple,  $\langle E, \oplus \rangle$ , where E is some type and  $\oplus$  is a "join" relation that satisfies functionality, associativity, commutativity, cancellation, self-join  $(a \oplus a = b \implies a = b)$ , and has a unit for each element  $(\forall a. \exists e. e \oplus a = a)$ .

We first define worlds, r, as a record of the heap (m), produce endpoints (p), and consume endpoints (c). These worlds and the join relation  $\oplus_w$  (rule Join-World in Figure 12) form a SA. Dockins et al. have shown how to construct a SA for the heap and  $\oplus_f$ ; we have constructed a SA for channel endpoints using the same approach, using the fact that  $\langle \mathsf{Endpoint}, \oplus_e \rangle$  is a SA.

A Share is the set of rationals over [0, 1]. The relation  $\oplus_s$  is the addition operator, and share  $\pi = 0$  is the unit for  $\oplus_s$ . A channel endpoint equal to Some  $(\pi, H)$  implies  $\pi > 0$ ; None implies a share of 0. In our notation, the produce history of channel d, in world r, is r.p(d).H; its share is  $r.p(d).\pi$ ; the consume history is r.c(d).H; and the consume share is  $r.c(d).\pi$ . (This notation implies that  $r.p(d) \neq$  None and  $r.c(d) \neq$  None). We write r.m(u) = Some v if the heap in world r contains value v at address u.

A HistorySet is a nonempty set of histories. The merge function ( $\mathbb{M}$ ) satisfies all the properties of a SA except self-join. Constructing a SA from the tuple of two SAs is straightforward, but without the property of self-join for  $\mathbb{M}$ , we must add the condition that for any Endpoint ( $\pi$ , H), if the share empty ( $\pi = 0$ ), then the set of histories is {nil}.

### 5.2 Predicate formulae

In Figure 13, we write  $\llbracket e \rrbracket_s$  to evaluate e within environment s, r[p: d+=v] to append value v to the local produce histories of channel d in r, and r[c: d+=v] to similarly update the local consume histories. An environment, s, is a finite partial map from variables to values.

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$r; s \models d_{\pi} H!$	iff	$r.p(d) = \text{Some } (\pi, \llbracket H \rrbracket_s) \land \forall d' \neq d. \ r.p(d') = \text{None}$
		$\wedge \forall d. \ r.c(d) = None \wedge \forall l. \ r.m(l) = None$
$r;s \models d_{\pi}H?$	iff	$r.c(d) = \text{Some } (\pi, \llbracket H \rrbracket_s) \land \forall d' \neq d. \ r.c(d') = \text{None}$
		$\wedge \forall d. r.p(d) = None \wedge \forall l. r.m(l) = None$
$r;s\models A[\mathbf{p}\!:d\!+\!\!=v]$	iff	$\exists r'. \ r = r'[\mathbf{p}: d + = v] \land r'; s \models A$
$r;s\models A[c:d{+}{=}v]$	iff	$\exists r'. \ r = r'[c: d + = v] \land r'; s \models A$
$r; s \models \text{PHist } d H$	iff	$r.p(d).H = \llbracket H \rrbracket_s$
$r; s \models \text{CHist } d H$	iff	$r.c(d).H = \llbracket H \rrbracket_s$
$r;s\models e_1\mapsto e_2$	iff	$r.m(\llbracket e_1 \rrbracket_s) = $ Some $\llbracket e_2 \rrbracket_s \land \forall l \neq \llbracket e_1 \rrbracket_s. r.m(l) = $ None
		$\wedge \forall d. r.p(d) = None \wedge r.c(d) = None$
$r;s \models A_1 * A_2$	iff	$\exists r_1, r_2. \ r_1 \oplus r_2 = r \wedge r_1; s \models A_1 \wedge r_2; s \models A_2$
$r;s \models A_1 \twoheadrightarrow A_2$	iff	$\forall r_1, r_2. \ r_1; s \models A_1 \implies r \oplus r_1 = r_2 \implies r_2; s \models A_2$
$r;s\models A_1\implies A_2$	iff	$r; s \models A_1 \implies r; s \models A_2$
$r;s\models e_1=e_2$	iff	$\llbracket e_1 \rrbracket_s = \llbracket e_2 \rrbracket_s$
$r;s\models emp$	iff	$\forall l. r.m(l) = None \land \forall d. r.p(d) = None \land r.c(d) = None$
	Б.	

Fig. 13: Predicate Formulae

### 5.3 Operational semantics

We present the operational semantics in Figure 14. The machine state is the tuple  $S = (\bar{c}, \bar{P})$ , where  $\bar{c}$  is a channel-indexed list of tuples which contain information about each channel's state. Specifically,  $\bar{c}[d] = (R, r, l_q, l_c)$ , where R is the resource invariant, r are the resources contained within the queue,  $l_q$  is the queue, and  $l_c$  is the list of consumed values.  $\bar{P}$  is a list of processes, where for any process  $k, \bar{P}[k] = (r, s, z), r$  are the process' resources, s is its environment, and z is the current instruction. Stepping process k from state S to state S' is written as  $S \rightarrow_k S'$ .

To produce a value, we use rule S-Produce. We start by appending the value,  $\llbracket e \rrbracket_s = v$ , to the local produce histories of the process' resources r, which we write as  $r[\mathbf{p}: d+=v]$ . Then, we push this value onto the back of the channel's queue,  $l_q$ . Finally, we split r into resources  $r_1$  and  $r_2$  such that  $r_1$  can be transferred to the channel while satisfying its resource invariant for the updated queue  $(v::l_q)$ , while the resources  $r_2$  remain with the producer.

We append the value to the producer's initial resources before splitting them because either  $r_1$  or  $r_2$  can record the value to its local produce history (although our Hoare rules currently prevent  $r_1$  from containing any history). The channel's resource invariant,  $\bar{R}[d]$ , is enough to determine  $r_1$  because we know that the updated channel is satisfied by  $r_q \oplus r_1$ ;  $\models \bar{R}[d](v::l_q, l_c)$  and that this resource invariant is precise (a requirement of  $\vdash \bar{R}[d]$  **R-okay**).

If consuming from a channel and its queue is empty, the consuming process will block (S-BlockingConsume). To progress using rule S-Consume, there must be a value v to receive from the front of the queue  $(l_q@v::nil)$  and we must show Concurrent Separation Logic for Pipelined Parallelization

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$$\begin{aligned} \frac{x \in \operatorname{dom}(s) \quad \tilde{P}[k] = (r, s, x: = e; \iota)}{(\bar{c}, \bar{P}) \rightarrow_k (\bar{c}, \bar{P}[k = (r, s[x = [e]_s], \iota)])} \text{ S-Assign} \\ \frac{x \in \operatorname{dom}(s) \quad \tilde{P}[k] = (r, s, x: = [e]_{+}\iota) \quad r.m([e]_s) = \operatorname{Some} v}{(\bar{c}, \bar{P}) \rightarrow_k (\bar{c}, \bar{P}[k = (r, s[x = v], \iota)])} \text{ S-Fetch} \\ \frac{\bar{P}[k] = (r, s, [e_1] := e_2; \iota) \quad r.m([e]_s) = \operatorname{Some} v}{(\bar{c}, \bar{P}) \rightarrow_k (\bar{c}, \bar{P}[k = (r, s, \texttt{vhile} e t; \iota')]} \text{ S-WhileTrue} \\ \frac{\bar{P}[k] = (r, s, [e_1] := e_2; \iota) \quad r.m([e]_s) = \operatorname{Some} v}{(\bar{c}, \bar{P}) \rightarrow_k (\bar{c}, \bar{P}[k = (r, s, \texttt{vhile} e t; \iota')]} \text{ S-WhileTrue} \\ \frac{[e]_s = true \quad \bar{P}[k] = (r, s, \texttt{vhile} e t; \iota')]}{(\bar{c}, \bar{P}) \rightarrow_k (\bar{c}, \bar{P}[k = (r, s, \texttt{vhile} e t; \iota')]} \text{ S-WhileFalse} \\ \frac{\bar{P}[k] = (r, s, \texttt{produce} d e; \iota) \quad \bar{C}[d] = (R, r_q, l_q, l_c)}{(\bar{c}, \bar{P}) \rightarrow_k (\bar{c}[d] = (R, r_q \oplus r_1, \upsilon); l_p; d \vdash v] = r_1 \oplus r_2} \quad [e]_s = v}{(\bar{c}, \bar{P}) \rightarrow_k (\bar{c}[d] = (R, r_q \oplus r_1, \upsilon); l_p; d \vdash v] = r_1 \oplus r_2} \\ \bar{P}[k] = (r, s, \texttt{consume} d x; \iota) \quad x \in \texttt{dom}(s) \\ \bar{C}[d] = (R, r_q, \theta; r_1, \upsilon); l_q; l_q; l_p; l_p; d \vdash v] s, s[x = v], \upsilon])} \end{array}$$
S-Consume   
$$\frac{\bar{P}[k] = (r, s, \texttt{consume} d x; \iota) \quad x \in \texttt{dom}(s)}{\bar{c}[d] = (R, r_q, l_q, l_c) \quad r_q; \vdash \bar{R}(l_q, \upsilon; l_c)]} \\ \bar{P}[k] = (r, s, \texttt{consume} d x; \iota) \quad r_q; \vdash \bar{R}(l_q, \upsilon; l_c)]} \\ \bar{P}[k] = (r, s, \texttt{consume} d x; \iota) \quad r_q; \vdash \bar{R}(l_q, \upsilon; l_c)] \\ \bar{C}, \bar{P} \rightarrow k (\bar{c}[d = (R, r_q, l_q, \upsilon; l_c)], \bar{P}[k = (r, s, l_q)]) \end{array}$$
S-Consume   
$$\frac{\bar{P}[k] = (r, s, \texttt{consume} d x; \iota) \quad \bar{C}[d] = (R, r_q, \texttt{ni}, l_c)}{(\bar{c}, \bar{P}) \rightarrow_k (\bar{c}, \bar{P}[k = (r, s, \texttt{sklp}; \iota)]} \\ S-BlockingConsume \\ \frac{\bar{P}[k] = (r, s, \texttt{consume} d x; \iota) \quad \bar{C}[d] = (R, r_q, \texttt{ni}, l_c)}{s_{z, q} = \texttt{dom}(s_0)} \\ \frac{\bar{P}[k] = (r, s, \texttt{assert} A; \iota) \quad r_s \mathrel{sklp} A + \texttt{strue}}{(\bar{c}, \bar{P}) \rightarrow_k (\bar{c}, \bar{P}[k = (r, s, \texttt{sklp}; \iota)]} \\ S-Assert \\ \frac{\bar{P}[k] = (r, s, [G_1; A_1] \ t \parallel [G_2; A_2] \ t_2; \iota) \quad \overset{s_1 \# s_2}{s_{z, q} = \texttt{dom}(s_0)} \\ r_1; \mathrel{s_1} \mathrel{s_1$$

$$\frac{I[k] = (I, S, \text{exit})}{(\bar{c}, \bar{P}) \to_k (\bar{c}, \bar{P})} \text{ S-Exit}$$

Fig. 14: Operational Semantics

that the channel's resource invariant will be satisfied by the channel's subsequent state. As a result, the consuming process receives the value and resources r', which are tied to the value, from the queue. The value is popped from the front of the queue and pushed onto the list of consumed values. Finally, the consumer's local histories are appended with the value  $((r \oplus r')[\mathbf{c}: d+=v])$  and the value is bound to the program variable x in the environment (s[x = v]).

Note that our operational semantics is not computable because we use logic formulae in the judgments. We believe that the forcing relationship can eventually be erased from our operational semantics during compilation.

Our operational semantics use permissions to guarantee that programs are well-synchronized, so that any process will get stuck if it attempts to access a resource without permission. Crucially, two processes may not have permission to mutate the same memory at the same time. Well-synchronized programs are race free, and it is generally understood that such programs have equivalent executions in both strong and weak memory models. Thus, while our operational semantics define a strong memory model, using a weak memory model would not change its behavior.

## 6 Soundness

We prove<sup>2</sup> soundness for our logic using progress and preservation. In our proofs, we consider only well-formed machine states S such that  $\vdash S$  well-formed. A well-formed machine state requires each channel state to satisfy its resource invariant; that the resource invariant R for each channel is  $\vdash R$  R-okay; that each process is well-formed; and that no two processes share any of the same environment variables. A process is well-formed only if its instructions have a Hoare triple derivation and if the precondition of this triple is exactly satisfied by the process' current resources and environment.

For any machine-states S and S',

**Theorem 2 (Preservation).** For all processes k, if  $\vdash S$  well-formed and  $S \rightarrow_k S'$ , then  $\vdash S'$  well-formed.

**Theorem 3 (Progress).** If  $\vdash S$  well-formed, then for all processes k, there either exists a state S' such that  $S \rightarrow_k S'$ , or process k in S is halted.

## 7 Related Work

Ottoni informally proved that when parallelizing a program, if the dependencies (the Program Dependency Graph) are preserved, then the generated program is observationally equivalent [10]. Yet this is not enough for a certified compiler because no implementation of the algorithm is proven.

Our CSL with channels was partially modeled after Concurrent C Minor [6]; specifically the style of resource invariants. There are close similarities between

<sup>&</sup>lt;sup>2</sup> Our proofs can be found at http://www.cs.princeton.edu/~cbell/cslchannels/

our while-programs with channels and pi-calculus, enough so that our CSL is similar to the logic proposed by Hoare and O'Hearn [5]. Turon et al. have extended that work with multiple producers and consumers [14] independently from us. Neither of these works have shared memory or an equivalent to histories, so are not applicable to reasoning about the correctness of DSWP.

Hurlin shows how to parallelize a sequential program's proof, using rewrite rules on its derivation tree, for the DOALL optimization [7]. We demonstrate how to prove a DSWP-parallelized program without using the proof's derivation tree, but we assume a proof structure that may not characterize all proofs.

## 8 Future Work & Conclusion

We have developed an operational semantics and CSL for asynchronous channels and proved the logic sound. This logic features histories that are used to overcome limitations in local reasoning and to prove the correctness of parallelized programs in the presence of asynchronous communication. We demonstrated how an existing proof of correctness (of a particular structure) for a sequential program can be used to generate a related proof for the parallelized output of DSWP. By maintaining the preconditions and postconditions, we can prove partial correctness of the optimization.

Our CSL and operational semantics are thus potential targets for an automatic method of generating parallelized proofs for parallelizing optimizations. Using such a method, we could prove that the optimization preserves all *specified* behaviors of a program.

First class channels are unnecessary for our proofs about DSWP. Some separation logics have first class objects [4][6], others do not permit passing objects this way [9]. We would need allocation, deallocation, and a more complicated definition of histories in order to support first class channels. The first two are not possible in first-order logic, but we believe it is straightforward to add following the approach used by Gotsman et al. and Hobor et al. The more complicated history model requires histories to have shared pasts that, upon merging, would retain their original ordering. For example, breaking the history {[123]} into histories {[12]} and {[3]} would result in {[123]} upon re-merging rather than {[123], [132], [312]}. (With such histories, side conditions involving PHist and CHist could be dropped from the Hoare rules).

We are now investigating methods of manipulating an existing arbitrary proof of a program using facts acquired from shape analysis, with the goal of eventually proving the correctness of DSWP and other parallelizing optimizations.

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