C6.2.5 ADD (shifted register)

Add (shifted register) adds a register value and an optionally-shifted register value, and writes the result to the destination register.

31	30	29	28	27	26	25	24	23 22	21	20 16	15	10	9 5	54	0
sf	0	0	0	1	0	1	1	shift	0	Rm	imm6		Rn		Rd
	ор	S													

32-bit variant

Applies when sf == 0.

ADD <Wd>, <Wn>, <Wm>{, <shift> #<amount>}

64-bit variant

Applies when sf == 1.

ADD <Xd>, <Xn>, <Xm>{, <shift> #<amount>}

Decode for all variants of this encoding

integer d = UInt(Rd); integer n = UInt(Rn); integer m = UInt(Rm); integer datasize = if sf == '1' then 64 else 32;

if shift == '11' then ReservedValue();
if sf == '0' && imm6<5> == '1' then ReservedValue();

ShiftType shift_type = DecodeShift(shift); integer shift_amount = UInt(imm6);

Assembler symbols

<wd></wd>	Is the 32-bit name of the general-purpose destination register, encoded in the "Rd" field.									
<wn></wn>	Is the 32-bit name of the first general-purpose source register, encoded in the "Rn" field.									
<\m>	Is the 32-bit name of the second general-purpose source register, encoded in the "Rm" field.									
<xd></xd>	Is the 64-bit name of the general-purpose destination register, encoded in the "Rd" field.									
<xn></xn>	Is the 64-bit name of the first general-purpose source register, encoded in the "Rn" field.									
<xm></xm>	Is the 64-bit name of the second general-purpose source register, encoded in the "Rm" field.									
<shift></shift>	Is the optional shift type to be applied to the second source operand, defaulting to LSL and encoded in the "shift" field. It can have the following values:									
	LSL when shift = 00									
	LSR when shift = 01									
	ASR when shift = 10									
	The encoding shift = 11 is reserved.									
<amount></amount>	For the 32-bit variant: is the shift amount, in the range 0 to 31, defaulting to 0 and encoded in the "imm6" field.									
	For the 64-bit variant: is the shift amount, in the range 0 to 63, defaulting to 0 and encoded in the "imm6" field.									

Operation

```
bits(datasize) result;
bits(datasize) operand1 = X[n];
bits(datasize) operand2 = ShiftReg(m, shift_type, shift_amount);
(result, -) = AddWithCarry(operand1, operand2, '0');
X[d] = result;
```