

Princeton University

COS 217: Introduction to Programming Systems

A Subset of IA-32 Assembly Language

Instruction Operands

Immediate Operands

Syntax: $\$i$

Semantics: Evaluates to i . Note that i could be a label...

Syntax: $\$label$

Semantics: Evaluates to the memory address denoted by $label$.

Register Operands

Syntax: $\%r$

Semantics: Evaluates to $\text{reg}[r]$, that is, the contents of register r .

Memory Operands

Syntax: $\%section:disp(\%base, \%index, scale)$

Semantics:

$section$ is a section register (CS, SS, DS, or ES).

$disp$ is a literal or label.

$base$ is a general-purpose register.

$index$ is any general purpose register except EBP.

$scale$ is the literal 2, 4, or 8.

One of $disp$, $base$, or $index$ is required. All other fields are optional.

Evaluates to the contents of memory at a certain address. That address consists of an offset into a section.

The section is specified by $section$. Assembly language programmers typically rely on the default section:

- CS for instruction fetches.
- SS for stack pushes and pops and references using ESP or EBP as base.
- DS for all data references except when relative to a stack or string destination.
- ES for the destinations of all string instructions.

The offset is computed using this expression:

$$\text{reg}[base] + (\text{reg}[index] * scale) + disp$$

The default $disp$ is 0. The default $scale$ is 0. If $base$ is omitted, then $\text{reg}[base]$ evaluates to 0. If $index$ is omitted, then $\text{reg}[index]$ evaluates to 0.

Commonly Used Memory Operands

Syntax	Semantics	Description
<i>label</i>	disp: <i>label</i> base: (none) index: (none) scale: (none) mem[0+(0*0)+ <i>label</i>] mem[<i>label</i>]	<p>Direct Addressing. The contents of memory at a certain address. The offset of that address is denoted by <i>label</i>.</p> <p>Often used to access a long, word, or byte in the bss, data, or rodata section.</p>
(% <i>r</i>)	disp: (none) base: <i>r</i> index: (none) scale: (none) mem[reg[<i>r</i>]+(0*0)+0] mem[reg[<i>r</i>]]	<p>Indirect Addressing. The contents of memory at a certain address. The offset of that address is the contents of register <i>r</i>.</p> <p>Often used to access a long, word, or byte in the stack section.</p>
<i>i</i> (% <i>r</i>)	disp: <i>i</i> base: <i>r</i> index: (none) scale: (none) mem[reg[<i>r</i>]+(0*0)+ <i>i</i>] mem[reg[<i>r</i>]+ <i>i</i>]	<p>Base-Pointer Addressing. The contents of memory at a certain address. The offset of that address is the sum of <i>i</i> and the contents of register <i>r</i>.</p> <p>Often used to access a long, word, or byte in the stack section.</p>
<i>label</i> (% <i>r</i>)	disp: <i>label</i> base: <i>r</i> index: (none) scale: (none) mem[reg[<i>r</i>]+(0*0)+ <i>label</i>] mem[reg[<i>r</i>]+ <i>label</i>]	<p>Indexed Addressing. The contents of memory at a certain address. The offset of that address is the sum of the address denoted by <i>label</i> and the contents of register <i>r</i>.</p> <p>Often used to access an array of bytes (characters) in the bss, data, or rodata section.</p>
<i>label</i> (,% <i>r</i> , <i>i</i>)	disp: <i>label</i> base: (none) index: <i>r</i> scale: <i>i</i> mem[0+(reg[<i>r</i>]* <i>i</i>)+ <i>label</i>] mem[(reg[<i>r</i>]* <i>i</i>)+ <i>label</i>]	<p>Indexed Addressing. The contents of memory at a certain address. The offset of that address is the sum of the address denoted by <i>label</i>, and the contents of register <i>r</i> multiplied by <i>i</i>.</p> <p>Often used to access an array of longs or words in the bss, data, or rodata section.</p>

Assembler Mnemonics

Key:

src: a source operand
dest: a destination operand
I: an immediate operand
R: a register operand
M: a memory operand
label: a label operand

For each instruction, at most one operand can be a memory operand.

Syntax	Semantics (expressed using C-like syntax)	Description
Data Transfer		
<code>mov{l,w,b} srcIRM, destRM</code>	$dest = src;$	Move. Copy <i>src</i> to <i>dest</i> .
<code>push{l,w} srcIRM</code>	$reg[ESP] = reg[ESP] - \{4,2\};$ $mem[reg[ESP]] = src;$	Push. Push <i>src</i> onto the stack.
<code>pop{l,w} destRM</code>	$dest = mem[reg[ESP]];$ $reg[ESP] = reg[ESP] + \{4,2\};$	Pop. Pop from the stack into <i>dest</i> .
<code>lea{l,w} srcM, destR</code>	$dest = \&src;$	Load Effective Address. Assign the address of <i>src</i> to <i>dest</i> .
<code>cld</code>	$reg[EDX:EAX] = reg[EAX];$	Convert Long to Double Register. Sign extend the contents of register EAX into the register pair EDX:EAX, typically in preparation for <code>idivl</code> .
<code>cwtd</code>	$reg[DX:AX] = reg[AX];$	Convert Word to Double Register. Sign extend the contents of register AX into the register pair DX:AX, typically in preparation for <code>idivw</code> .
<code>cbtw</code>	$reg[AX] = reg[AL];$	Convert Byte to Word. Sign extend the contents of register AL into register AX, typically in preparation for <code>idivb</code> .
<code>leave</code>	Equivalent to: <code>movl %ebp, %esp</code> <code>popl %ebp</code>	Pop a stack frame in preparation for leaving a function
Arithmetic		
<code>add{l,w,b} srcIRM, destRM</code>	$dest = dest + src;$	Add. Add <i>src</i> to <i>dest</i> .
<code>sub{l,w,b} srcIRM, destRM</code>	$dest = dest - src;$	Subtract. Subtract <i>src</i> from <i>dest</i> .
<code>inc{l,w,b} destRM</code>	$dest = dest + 1;$	Increment. Increment <i>dest</i> .
<code>dec{l,w,b} destRM</code>	$dest = dest - 1;$	Decrement. Decrement <i>dest</i> .
<code>neg{l,w,b} destRM</code>	$dest = -dest;$	Negate. Negate <i>dest</i> .
<code>imull srcRM</code>	$reg[EDX:EAX] = reg[EAX] * src;$	Signed Multiply. Multiply the contents of register EAX by <i>src</i> , and store the product in registers EDX:EAX.
<code>imulw srcRM</code>	$reg[DX:AX] = reg[AX] * src;$	Signed Multiply. Multiply the contents of register AX by <i>src</i> , and store the product in registers DX:AX.
<code>imulb srcRM</code>	$reg[AX] = reg[AL] * src;$	Signed Multiply. Multiply the contents of register AL by <i>src</i> , and store the product in AX.
<code>idivl srcRM</code>	$reg[EAX] = reg[EDX:EAX] / src;$ $reg[EDX] = reg[EDX:EAX] \% src;$	Signed Divide. Divide the contents of registers EDX:EAX by <i>src</i> , and store the quotient in register EAX and the remainder in register EDX.

<code>idivw srcRM</code>	<code>reg[AX] = reg[DX:AX]/src;</code> <code>reg[DX] = reg[DX:AX]%src;</code>	Signed Divide. Divide the contents of registers DX:AX by <i>src</i> , and store the quotient in register AX and the remainder in register DX.
<code>idivb srcRM</code>	<code>reg[AL] = reg[AX]/src;</code> <code>reg[AH] = reg[AX]%src;</code>	Signed Divide. Divide the contents of register AX by <i>src</i> , and store the quotient in register AL and the remainder in register AH.
<code>mull srcRM</code>	<code>reg[EDX:EAX] = reg[EAX]*src;</code>	Unsigned Multiply. Multiply the contents of register EAX by <i>src</i> , and store the product in registers EDX:EAX.
<code>mulw srcRM</code>	<code>reg[DX:AX] = reg[AX]*src;</code>	Unsigned Multiply. Multiply the contents of register AX by <i>src</i> , and store the product in registers DX:AX.
<code>mulb srcRM</code>	<code>reg[AX] = reg[AL]*src;</code>	Unsigned Multiply. Multiply the contents of register AL by <i>src</i> , and store the product in AX.
<code>divl srcRM</code>	<code>reg[EAX] = reg[EDX:EAX]/src;</code> <code>reg[EDX] = reg[EDX:EAX]%src;</code>	Unsigned Divide. Divide the contents of registers EDX:EAX by <i>src</i> , and store the quotient in register EAX and the remainder in register EDX.
<code>divw srcRM</code>	<code>reg[AX] = reg[DX:AX]/src;</code> <code>reg[DX] = reg[DX:AX]%src;</code>	Unsigned Divide. Divide the contents of registers DX:AX by <i>src</i> , and store the quotient in register AX and the remainder in register DX.
<code>divb srcRM</code>	<code>reg[AL] = reg[AX]/src;</code> <code>reg[AH] = reg[AX]%src;</code>	Unsigned Divide. Divide the contents of register AX by <i>src</i> , and store the quotient in register AL and the remainder in register AH.
Bitwise		
<code>and{l,w,b} srcIRM, destRM</code>	<code>dest = dest & src;</code>	And. Bitwise and <i>src</i> into <i>dest</i> .
<code>or{l,w,b} srcIRM, destRM</code>	<code>dest = dest src;</code>	Or. Bitwise or <i>src</i> into <i>dest</i> .
<code>xor{l,w,b} srcIRM, destRM</code>	<code>dest = dest ^ src;</code>	Exclusive Or. Bitwise exclusive or <i>src</i> into <i>dest</i> .
<code>not{l,w,b} destRM</code>	<code>dest = ~dest;</code>	Not. Bitwise not <i>dest</i> .
<code>sal{l,w,b} srcIR, destRM</code>	<code>dest = dest << src;</code>	Shift Arithmetic Left. Shift <i>dest</i> to the left <i>src</i> bits, filling with zeros.
<code>sar{l,w,b} srcIR, destRM</code>	<code>dest = dest >> src;</code>	Shift Arithmetic Right. Shift <i>dest</i> to the right <i>src</i> bits, sign extending the number.
<code>shl{l,w,b} srcIR, destRM</code>	(Same as <code>sal</code>)	Shift Left. (Same as <code>sal</code> .)
<code>shr{l,w,b} srcIR, destRM</code>	(Same as <code>sar</code>)	Shift Right. Shift <i>dest</i> to the right <i>src</i> bits, filling with zeros.
Control Transfer		
<code>cmp{l,w,b} srcIRM1,srcRM2</code>	<code>reg[EFLAGS] =</code> <code>srcRM2 comparedwith srcIRM1</code>	Compare. Compare <i>src2</i> with <i>src1</i> , and set the condition codes in the EFLAGS register accordingly.
<code>jmp label</code>	<code>reg[EIP] = label;</code>	Jump. Jump to <i>label</i> .
<code>j{e,ne} label</code>	<code>if (reg[EFLAGS] appropriate)</code> <code>reg[EIP] = label;</code>	Conditional Jump. Jump to <i>label</i> iff the condition codes in the EFLAGS register indicate an equality or inequality (respectively) relationship between the most recently compared numbers.
<code>j{l,le,g,ge} label</code>	<code>if (reg[EFLAGS] appropriate)</code> <code>reg[EIP] = label;</code>	Signed Conditional Jump. Jump to <i>label</i> iff the condition codes in the EFLAGS register indicate a less than, less than or equal to, greater than, or greater than or equal to (respectively) relationship between the most recently compared numbers.
<code>j{b,be,a,ae} label</code>	<code>if (reg[EFLAGS] appropriate)</code> <code>reg[EIP] = label;</code>	Unsigned Conditional Jump. Jump to <i>label</i> iff the condition codes in the EFLAGS register indicate a below, below

		or equal to, above, or above or equal to (respectively) relationship between the most recently compared numbers.
call <i>label</i>	reg[ESP] = reg[ESP] - 4; mem[reg[ESP]] = reg[EIP]; reg[EIP] = <i>label</i> ;	Call. Call the function that begins at <i>label</i> .
call * <i>srcR</i>	reg[ESP] = reg[ESP] - 4; mem[reg[ESP]] = reg[EIP]; reg[EIP] = reg[<i>srcR</i>];	Call. Call the function whose address is in <i>src</i> .
ret	reg[EIP] = mem[reg[ESP]]; reg[ESP] = reg[ESP] + 4;	Return. Return from the current function.
int <i>srcIRM</i>	Generate interrupt number <i>src</i>	Interrupt. Generate interrupt number <i>src</i> .

Assembler Directives

Syntax	Description
<i>label</i> :	Record the fact that <i>label</i> marks the current location within the current section
.section " <i>sectionname</i> "	Make the <i>sectionname</i> section the current section
.skip <i>n</i>	Skip <i>n</i> bytes of memory in the current section
.align <i>n</i>	Skip as many bytes of memory in the current section as necessary so the current location is evenly divisible by <i>n</i>
.byte <i>bytevalue1</i> , <i>bytevalue2</i> , ...	Allocate one byte of memory containing <i>bytevalue1</i> , one byte of memory containing <i>bytevalue2</i> , ... in the current section
.word <i>wordvalue1</i> , <i>wordvalue2</i> , ...	Allocate two bytes of memory containing <i>wordvalue1</i> , two bytes of memory containing <i>wordvalue2</i> , ... in the current section
.long <i>longvalue1</i> , <i>longvalue2</i> , ...	Allocate four bytes of memory containing <i>longvalue1</i> , four bytes of memory containing <i>longvalue2</i> , ... in the current section
.ascii " <i>string1</i> ", " <i>string2</i> ", ...	Allocate memory containing the characters from <i>string1</i> , <i>string2</i> , ... in the current section
.asciz " <i>string1</i> ", " <i>string2</i> ", ...	Allocate memory containing <i>string1</i> , <i>string2</i> , ..., where each string is NULL terminated, in the current section
.string " <i>string1</i> ", " <i>string2</i> ", ...	(Same as .asciz)
.globl <i>label1</i> , <i>label2</i> , ...	Mark <i>label1</i> , <i>label2</i> , ... so they are available to the linker
.equ <i>name</i> , <i>expr</i>	Define <i>name</i> as a symbolic alias for <i>expr</i>
.lcomm <i>label</i> , <i>n</i> [, <i>align</i>]	Allocate <i>n</i> bytes, marked by <i>label</i> , in the bss section [and align the bytes on an <i>align</i> -byte boundary]
.comm <i>label</i> , <i>n</i> , [, <i>align</i>]	Allocate <i>n</i> bytes, marked by <i>label</i> , in the bss section, mark label so it is available to the linker [and align the bytes on an <i>align</i> -byte boundary]
.type <i>label</i> ,@function	Mark <i>label</i> so the linker knows that it denotes the beginning of a function