An Analysis of Pipeline Clocking

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Abstract

This note examines timing constraints on latches in pipelined systems. The goal is to determine required clock characteristics based on pipeline parameters such as gate delays (both max and min), signal delays, and the number of logic levels. Both single and multi-phase clocks are considered.

1. Introduction

The analysis is based on the simple latch design illustrated in Fig. 1. Clock waveforms for C and $\overline{C}$ are illustrated in Fig. 2. These two clock waveforms are the complements of one another, intentionally skewed slightly. The reason for this skew will be described shortly. Throughout the analysis it is assumed that the width of the C_{high} pulse is the same as the width of the $\overline{C}_{low}$ pulse.

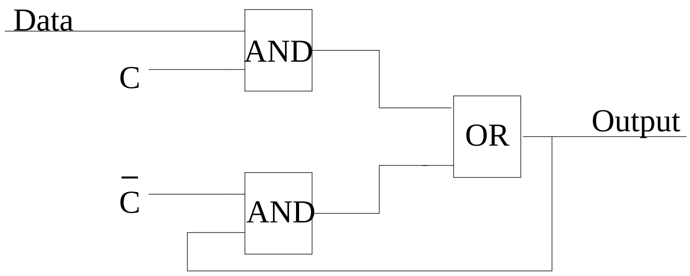


Fig. 1. Latch to be analyzed.

Our initial analysis assumes that the logic used for clock fanout has no unintentional skew due to gate delay differences. That is, clock signals reaching the latches are perfectly controlled.

The distinction between intentional skew and unintentional skew should be noted. It is often necessary to intentionally skew clock signals. This is done in the case of multi-phase clocks, and in controlling the C and $\overline{C}$ signals to avoid hazards. Unintentional skew is due to imperfections in the clock distribution network and fanout logic. Initially, unintentional skews are ignored to simplify the analysis. Then, later analysis takes the effects of unintentional skews into account.

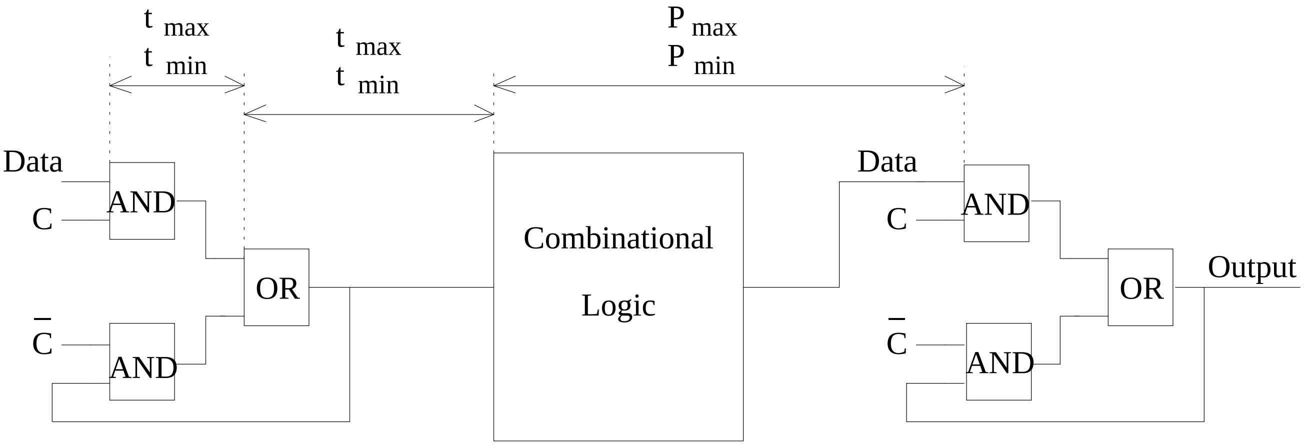
The following notation is used.

- $t_{\max}$ - maximum propagation delay time for a logic level
- $t_{\min}$ - minimum propagation delay time for a logic level
- C_{high} - the duration of C = 1 (clock high)
- C_{low} - the duration of C = 0 (clock low)
- $P_{\max}$ - maximum delay time on the maximum delay path from the output of a latch to input of the next latch. This includes all the delay due to combinational logic between latches, but does not include delay for the latches.
- $P_{\min}$ - minimum delay time on the minimum delay path from the output of a latch to input of the next latch.

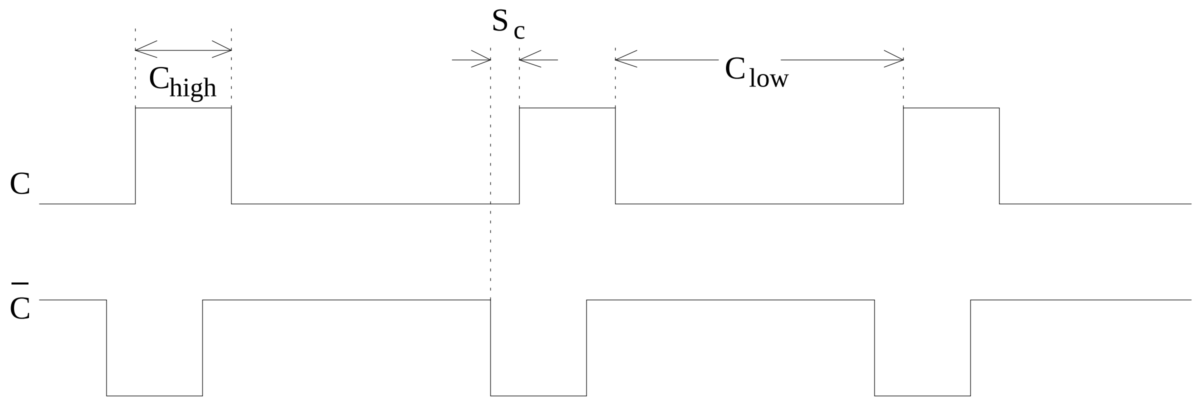
S_c - The skew between the $\bar{C}$ and C clock signals. This skew is to avoid logic hazards and is positive.

S_p - The skew between two consecutive clock phases of a multi-phased clock. This skew is the time that the second clock phase is delayed with respect to the first.

U_X - This is used to represent unintentional skews and is the uncertainty of X. It represents the quantity such that X lies in the interval $(X - U_X,\ X + U_X)$.



(a)



(b)

Fig. 2. Illustration of timing parameters.
(a) Logic delay parameters
(b) Clock parameters

Fig. 2 illustrates several of the above timing parameters. S_p is shown in Fig. 3. In the discussion when "gate delays" are referred to, signal propagation and loading delays are also included. They are assumed to be modeled as part of the delay associated with the driving gate, as shown in Fig. 2.

2. Single Phase Clocks

2.1. Basic Timing Constraints

There are four basic timing constraints on the clock signals for a single phase clocking system. For simplicity, unintentional skews are ignored in this section.

(1) **The skew constraint:** S_c must be at least $t_{\max} - t_{\min}$. Otherwise, C falling (and being propagated in time $t_{\min}$ through the upper AND gate in Fig. 1) may cause a glitch at the latch output because the rise of $\bar{C}$ propagating through the lower AND gate may take as long as $t_{\max}$. This glitch will result in unreliable latching of data.

$$S_c \geq t_{\max} - t_{\min}. \qquad (1)$$

(2) **The latching constraint:** The clock pulse C_{high} has to be wide enough to ensure that valid data is captured in the latch. That is, it must be wide enough to allow data to propagate from the D input to the latch output, then to feed back around to be latched by the $\bar{C}$ signal. The maximum propagation delay from the input of the latch to the output once C has gone high is $2t_{\max}$. In addition, the time needed to ensure that the feedback from the output will hold the latch is $t_{\max} - t_{\min}$. This gives

$$C_{high} \geq 3t_{\max} - t_{\min}. \qquad (2)$$

(3) **The short-path constraint:** The maximum width of the clock pulse, C_{high}, must be shorter than the minimum propagation delay from the input of one latch to the input of the next, assuming no intentional clock skew. Otherwise, a value at a latch's input will be propagated through the latch and make it to the input of the next latch (and possibly be latched there) during a single clock pulse. The minimum time to propagate a signal through the latch and through the intervening logic to the next latch is $2t_{\min} + P_{\min}$ (the latch delay plus the combinational logic delay) To get the proper constraint, observe that the output of a latch is first affected by the fall in the C input, and it is actually this change which starts the worst-case minimum delay path. Hence, the skew S_c further reduces the minimum propagation delay path.

$$C_{high} \leq 2t_{\min} + P_{\min} - S_c \qquad (3)$$

(4) **The long-path constraint:** A latch cannot be clocked until the data from the previous latch has arrived. Thus the minimum clock period, $C_{high} + C_{low}$, must be longer than the maximum propagation delay from the input of one latch to the input of the following latch. The complete expression is

$$C_{high} + C_{low} \geq 2t_{\max} + P_{\max}. \qquad (4)$$

2.2. Derived Properties and Observations

From the above basic clock constraints, some additional clock properties can be derived. First, (2) and (3) can be combined (because (3) upper bounds C_{high} and (2) lower bounds it):

$$2t_{\min} + P_{\min} - S_c \geq 3t_{\max} - t_{\min}.$$

This equation can be solved for $P_{\min}$:

$$P_{\min} \geq 3t_{\max} - 3t_{\min} + S_c.$$

Now substituting for S_c using (1):

$$P_{\min} \geq 4t_{\max} - 4t_{\min}. \qquad (5)$$

For reliable operation, the minimum inter-latch logic delay must be at least equal to the "data skews" through four gates, where the data skew is the maximum gate delay minus the minimum gate delay.

Continue this analysis by defining r to be the ratio of the minimum gate delay to the maximum, and n to be the number of gate levels between latches. ($n+2$ gate levels including the two in the latch). $t_{\min} = rt_{\max}$. Substituting $rt_{\max}$ for $t_{\min}$ and $nrt_{\max}$ for $P_{\min}$ and rearranging yields

$$n \geq \frac{4}{r} - 4 \tag{6}$$

That is, for a single phase clock there must be at least $n \geq \frac{4}{r} - 4$ gate levels for proper operation. If the number of gate levels is fewer, then some extra delay must be intentionally added. For example, if $r = .5$, $n \geq 4$, which implies there must be at least enough delay for 4 logic levels between latches, 6 including the two in the latch, itself.

It is also possible to derive an expression for the clock period in terms of the gate data skews. To do this, rewrite (4):

$$C_{high} + C_{low} \geq 2t_{\max} + P_{\max} - P_{\min} + P_{min.}$$

and then substituting (5) for the last instance of $P_{\min}$:

$$C_{high} + C_{low} \geq 6t_{\max} - 4t_{\min} + P_{\max} - P_{\min}. \tag{7}$$

Again, let n be the number of inter-latch gate levels, then (7) can be re-written as:

$$C_{high} + C_{low} \geq 2t_{\max} + (n+4)(t_{\max} - t_{\min}). \tag{8}$$

That is, the minimum clock period is two maximum gate delays plus $n + 4$ gate data skews. Of course the clock period must also satisfy the long-path constraint (4).

3. Multi-Phase Clocks

3.1. Basic Timing Constraints

With a multiphase clock, the clock signals feeding two consecutive latches, i-1 and i, are skewed by a constant amount with respect to one another. Let S_p represent this "phasing" skew. S_p is the time difference between a clock pulse at latch i-1 and the next clock pulse at latch i. This is shown in Fig. 3. The four basic timing constraints follow. The first two are the same as for a single phase clock, but are repeated for completeness.

(1) **The clock skew constraint:**

$$S_c \geq t_{\max} - t_{\min}. \tag{9}$$

(2) **The latching constraint:**

$$C_{high} \geq 3t_{\max} - t_{\min}. \tag{10}$$

(3) **The short-path constraint:** Using phased clocks relaxes the short-path constraint. The clock pulse may be wider by an amount equal to the entire clock period, $C_{high} + C_{low}$, minus the phasing skew, S_p.

$$C_{high} \leq 2t_{\min} + P_{\min} - S_c + (C_{high} + C_{low} - S_p) \tag{11}$$

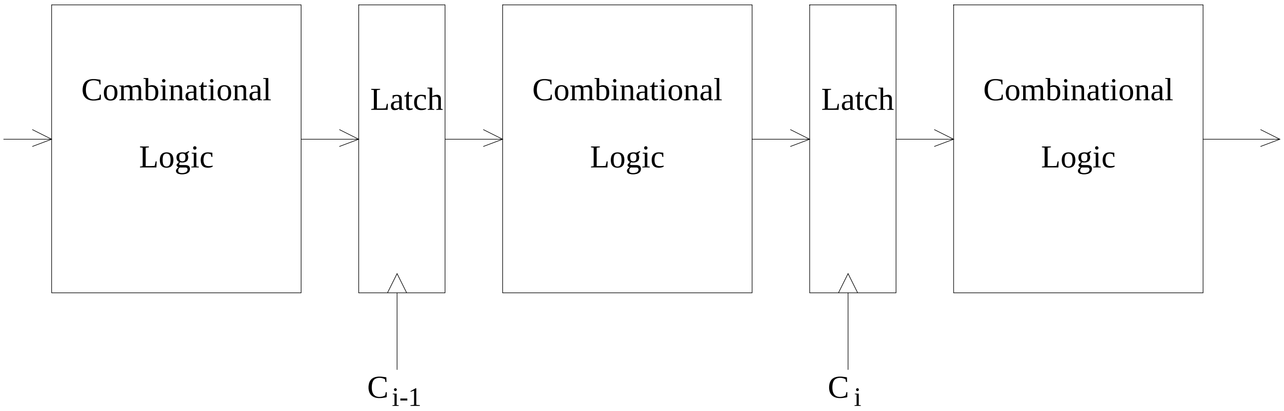
(4) **The long-path constraint:** As before, a latch cannot be clocked until the data from the previous latch has arrived. Now, however, the data from the previous latch arrives at time S_p, so:

$$S_p \geq 2t_{\max} + P_{\max}. \tag{12}$$

As before, additional clock properties can be derived. A bound on $P_{\min}$ can be derived in a similar way to (5):

$$P_{\min} \geq 4t_{\max} - 4t_{\min} - (C_{high} + C_{low} - S_p). \tag{13}$$

In most cases, the clock period minus S_p will be bigger than four gate delay skews. When this is true there is effectively no limit on $P_{\min}$; it can be zero.



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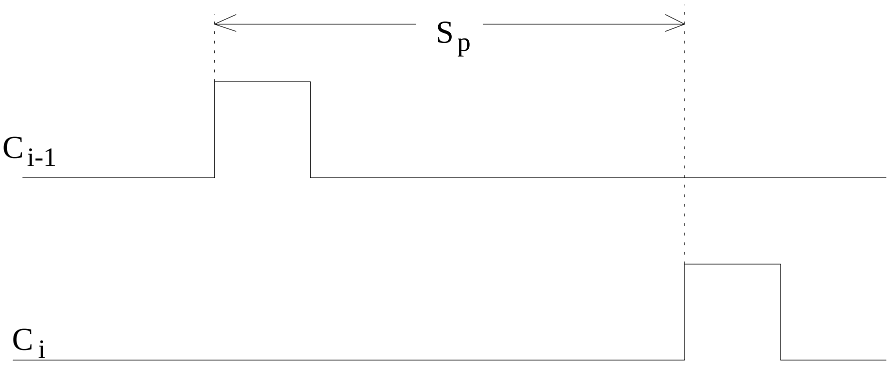

(b)

Fig. 3. Illustration of multiple phase clocks ($\bar{C}$ clocks not shown).
(a) Latch stages i-1 and i
(b) Phasing skew, S_p

It is also possible to derive an expression for the clock period. First, rearrange (13):

$$C_{high} + C_{low} \geq 4t_{\max} - 4t_{\min} - P_{\min} + S_p.$$

Then, (12) is substituted for S_p to yield:

$$C_{high} + C_{low} \geq 6t_{\max} - 4t_{\min} + P_{\max} - P_{\min}. \tag{14}$$

Observe that this bound on the clock period is exactly the same as with a single-phase clock. This indicates that a multiple phase clock doesn't necessarily lead to a faster system; its primary advantage is in relaxing the short-path constraint on C_{high}.

3.2. Two-phase clock

Assume a two phase clock where S_p is exactly half the clock period. The first two basic clock constraints do not involve S_p, and are therefore unchanged. The short-path constraint, (11), can be re-written as:

$$C_{high} \leq 2t_{\min} + P_{\min} - S_c + (C_{high} + C_{low})/2 \tag{15}$$

That is, for a two phase clock, C_{high} can be a half clock period wider than with a single phase clock. Hence, unless a very wide clock pulses are used, short paths cease to be a problem.

The long-path constraint (12) can be re-written as:

$$C_{high} + C_{low} \geq 4t_{\max} + 2P_{\max}. \tag{16}$$

That is, the clock period must accommodate two phases worth of latches and logic (not exactly an earth-shaking observation, but re-assuring).

4. Unintentional Clock Skew

The results in the previous section are based on an assumption of a perfectly controlled clock. To model more realistic systems, it is necessary to add uncertainty terms to the clocking constraints.

Assume there can be unintentional skew between the C and $\overline{C}$ signals (denoted as $U_{C,\overline{C}}$), between clock signals reaching different latches (U_{C_{i-1},C_i}), and there can be uncertainty in the pulse width ($U_{C_{high}}$). It is assumed that the unintentional skews are not correlated. Expressions with uncertainty terms added are derived in a manner very similar to (1) through (16); to show the correspondence with the previous expressions, they are denoted as (1*) to (16*).

4.1. Basic Clocking Constraints

With unintentional skews added, the four clock constraints, for a single phase clock become:

(1) **The skew constraint:**

$$S_c \geq t_{\max} - t_{\min} + U_{C,\overline{C}}. \tag{1*}$$

(2) **The latching constraint:**

$$C_{high} \geq 3t_{\max} - t_{\min} + U_{C_{high}}. \tag{2*}$$

(3) **The short-path constraint:**

$$C_{high} \leq 2t_{\min} + P_{\min} - S_c - U_{C,\overline{C}} - U_{C_{i-1},C_i} - U_{C_{high}}. \tag{3*}$$

(4) **The long-path constraint:**

$$C_{high} + C_{low} \geq 2t_{\max} + P_{\max} + U_{C_{i-1},C_i}. \tag{4*}$$

Combining (2*) and (3*) and solving for $P_{\min}$, and substituting (1*) yields:

$$P_{\min} \geq 4t_{\max} - 4t_{\min} + U_{C_{i-1},C_i} + 2U_{C,\overline{C}} + 2U_{C_{high}}. \tag{5*}$$

Using r as the ration of $t_{\min}$ to $t_{\max}$ and n as the number of logic levels between latches, yields the bound on n:

$$n \geq \frac{4}{r} - 4 + \frac{U_{C_{i-1},C_i} + 2U_{C,\overline{C}} + 2U_{C_{high}}}{t_{\min}} \tag{6*}$$

Continuing on, the bounds on the clock period are:

$$C_{high} + C_{low} \geq 6t_{\max} - 4t_{\min} + P_{\max} - P_{\min} + U_{C_{i-1},C_i} + 2U_{C,\overline{C}} + 2U_{C_{high}}. \tag{7*}$$

$$C_{high} + C_{low} \geq 2t_{\max} + (n+4)(t_{\max} - t_{min)} + U_{C_{i-1},C_i} + 2U_{C,\overline{C}} + 2U_{C_{high}}. \tag{8*}$$

Using the same methods as before, the equations for a multi-phase clock with unintentional skews follow.

The clock skew constraint:

$$S_c \geq t_{\max} - t_{\min} + U_{C,\bar{C}}. \tag{9*}$$

The latching constraint:

$$C_{high} \geq 3t_{\max} - t_{\min} + U_{C_{high}}. \tag{10*}$$

The short-path constraint:

$$C_{high} \leq 2t_{\min} + P_{\min} - S_c + (C_{high} + C_{low} - S_p) - U_{C,\bar{C}} - U_{C_{i-1},C_i} - U_{C_{high}}. \tag{11*}$$

The long-path constraint:

$$S_p \geq 2t_{\max} + P_{\max} + U_{C_{i-1},C_i}. \tag{12*}$$

For multiple phase clocks with unintentional skews added, clock relationships derived from the four constraints follow.

$$P_{\min} \geq 4t_{\max} - 4t_{\min} - (C_{high} + C_{low} - S_p) + U_{C_{i-1},C_i} + 2U_{C,\bar{C}}. \tag{13*}$$

$$C_{high} + C_{low} \geq 6t_{\max} - 4t_{\min} + P_{\max} - P_{\min} + U_{C_{i-1},C_i} + 2U_{C,\bar{C}} + 2U_{C_{high}}. \tag{14*}$$

$$C_{high} \leq 2t_{\min} + P_{\min} - S_c + (C_{high} + C_{low})/2 - U_{C,\bar{C}} - U_{C_{i-1},C_i} - U_{C_{high}}. \tag{15*}$$

$$C_{high} + C_{low} \geq 4t_{\max} + 2P_{\max} + 2U_{C_{i-1},C_i}. \tag{16*}$$

5. Bibliography

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