STRB (immediate)

Store Register Byte (immediate) stores the least significant byte of a 32-bit register to memory. The address that is used for the store is calculated from a base register and an immediate offset. For information about memory accesses, see Load/Store addressing modes on page C1-149.

Post-index

<table>
<thead>
<tr>
<th>0 0</th>
<th>1 1</th>
<th>1 1</th>
<th>0 0</th>
<th>0 0</th>
<th>0 0</th>
<th>imm9</th>
<th>0 1</th>
<th>Rn</th>
<th>Rt</th>
</tr>
</thead>
<tbody>
<tr>
<td>size</td>
<td>opc</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Post-index variant

STRB <Wt>, [<Xn|SP>], #<simm>

Decode for this encoding

boolean wback = TRUE;
boolean postindex = TRUE;
bits(64) offset = SignExtend(imm9, 64);

Pre-index

<table>
<thead>
<tr>
<th>0 0</th>
<th>1 1</th>
<th>1 1</th>
<th>0 0</th>
<th>0 0</th>
<th>0 0</th>
<th>imm9</th>
<th>1 1</th>
<th>Rn</th>
<th>Rt</th>
</tr>
</thead>
<tbody>
<tr>
<td>size</td>
<td>opc</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Pre-index variant

STRB <Wt>, [<Xn|SP>, #<simm>]

Decode for this encoding

boolean wback = TRUE;
boolean postindex = FALSE;
bits(64) offset = SignExtend(imm9, 64);

Unsigned offset

<table>
<thead>
<tr>
<th>0 0</th>
<th>1 1</th>
<th>1 1</th>
<th>0 0</th>
<th>0 1</th>
<th>0 0</th>
<th>imm12</th>
<th>Rn</th>
<th>Rt</th>
</tr>
</thead>
<tbody>
<tr>
<td>size</td>
<td>opc</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Unsigned offset variant

STRB <Wt>, [<Xn|SP>{, #pimm}]

Decode for this encoding

boolean wback = FALSE;
boolean postindex = FALSE;
bits(64) offset = LSL(ZeroExtend(imm12, 64), 0);
Notes for all encodings

For information about the CONstrained UNPREDICTable behavior of this instruction, see Appendix K1 Architectural Constraints on UNPREDICTABLE behaviors, and particularly STRB (immediate) on page K1-6425.

Assembler symbols

<\!t> Is the 32-bit name of the general-purpose register to be transferred, encoded in the "Rt" field.

<Xn|SP> Is the 64-bit name of the general-purpose base register or stack pointer, encoded in the "Rn" field.

<\!imm> Is the signed immediate byte offset, in the range -256 to 255, encoded in the "imm9" field.

<\!pimm> Is the optional positive immediate byte offset, in the range 0 to 4095, defaulting to 0 and encoded in the "imm12" field.

Shared decode for all encodings

integer n = UInt(Rn);
integer t = UInt(Rt);

Operation for all encodings

bits(64) address;
bits(8) data;
boolean rt_unknown = FALSE;

if wback && n == t && n != 31 then
  c = ConstrainUnpredictable();
  assert c IN {Constraint_NONE, Constraint_UNKNOWN, Constraint_UNDEF, Constraint_NOP};
  case c of
    when Constraint_NONE rt_unknown = FALSE; // value stored is original value
    when Constraint_UNKNOWN rt_unknown = TRUE; // value stored is UNKNOWN
    when Constraint_UNDEF UnallocatedEncoding();
    when Constraint_NOP EndOfInstruction();
  end case;

if n == 31 then
  CheckSPAlignment();
  address = SP[ ];
else
  address = X[n];

if !postindex then
  address = address + offset;

if rt_unknown then
  data = bits(8) UNKNOWN;
else
  data = X[t];
Mem[address, 1, AccType_NORMAL] = data;

if wback then
  if postindex then
    if n == 31 then
      SP[ ] = address;
    else
      X[n] = address;