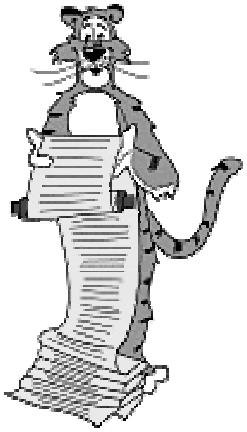
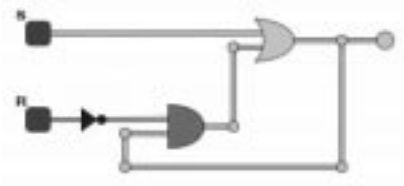
Lecture A4: Sequential Circuits





Architecture

Lecture A1 – A2: TOY machine.

Lecture A3: Boolean logic and combinational circuits.

- In principle, we could build TOY computer with one gigantic combinational circuit.
- Each circuit element used (at most) once.

Today.

- How to reuse circuit elements.
- How to store bits of information in memory.

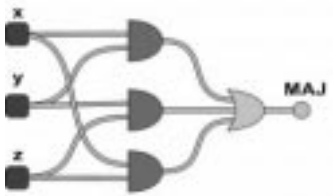
Next time.

- Glue these components into a TOY computer.

Sequential vs. Combinational Circuits

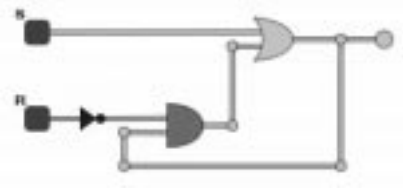
Combinational circuits.

- Output determined solely by inputs.



Sequential circuits.

- Feedback loop.
- Output determined by inputs and previous outputs.



Flip-Flop

Flip-flop.

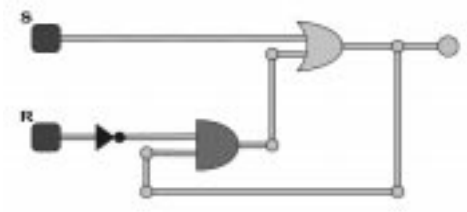
- A smallest sequential circuit.
- Can "remember" one bit of information.

We will consider many flavors.

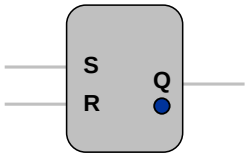
SR Flip-Flop

SR Flip-Flop.

- Pulse on S (set) ⇒ line turns flip-flop on.
- Pulse on R (reset) ⇒ line turns flip-flop off.
- S = R = 0 ⇒ line
- S = R = 1 ⇒ not allowed



Implementation



Interface

Truth Table and Timing Diagram (for SR Flip-Flop)

Truth table.

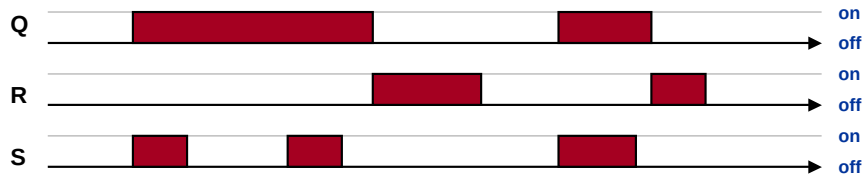
- Values vary over time.
- S(t), R(t), Q(t) denote value at time t.

SR Flip Flop Truth Table			
S(t)	R(t)	Q(t)	Q(t+ε)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	
1	1	1	

Characteristic equation.

$$Q(t+\varepsilon) = S(t) + R'(t)Q(t) \qquad (SR = 0)$$

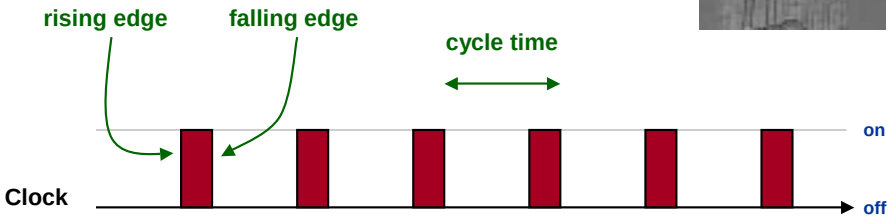
Sample timing diagram.



Clock

Clock.

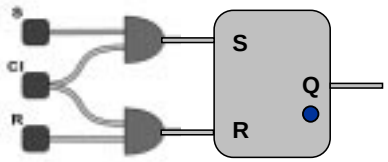
- Regular on-off pulse.
- Synchronize operations of different circuit elements.
- 800 MHz clock means 800 million pulses per second.



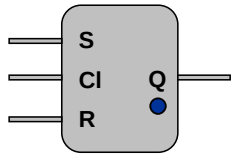
Clocked SR Flip-Flop

Clocked SR Flip-Flop.

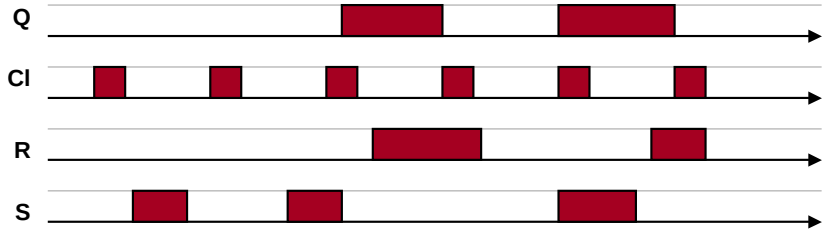
- Like SR flip-flop but S and R only work if clock is on.



Implementation



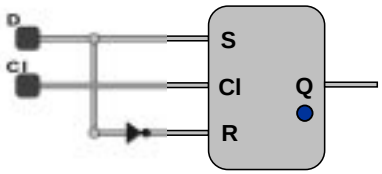
Interface



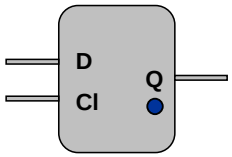
Clocked D Flip-Flop

Clocked D Flip-Flop.

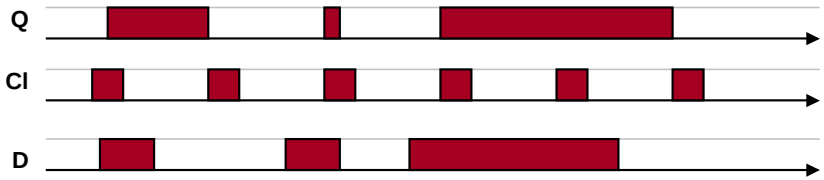
- On clock pulse: if D = 1, then set; if D = 0, then reset



Implementation



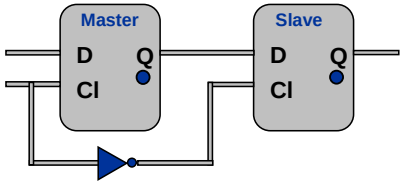
Interface

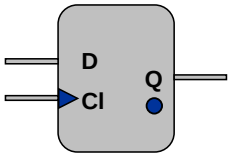


Master Slave Flip-Flop

Master-slave flip-flop (falling edge-trigger).

- Input can only change on falling edge.



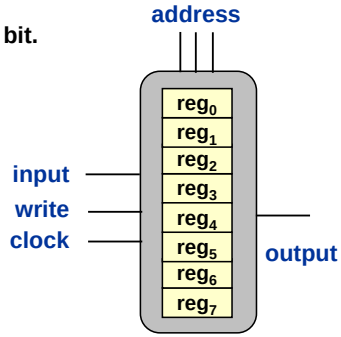


Interface

Register File (bits)

Register file: n bits.

- n bits to choose from.
- Address specifies which bit.
  - How many bits needed to specify address?
- If write = 1, input gets copied into chosen bit.
- If write = 0, chosen bit appears on output.

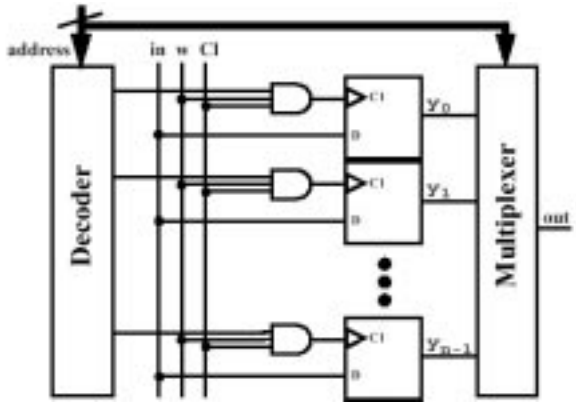


Interface
(8 bits)

Register File (bits)

Register file: n bits.

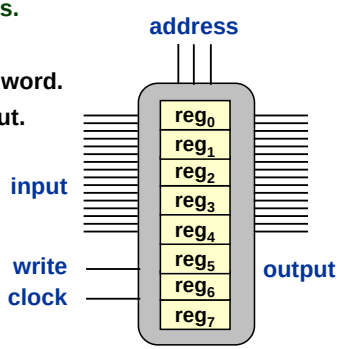
- Decoder writes input to address bit.
- Multiplexer copies address bit to output.



Register File (words)

Register file: n registers (words), k bits per register.

- n k-bit words to choose from.
  - TOY main memory: 256 16-bit words.
  - TOY registers: 8 16-bit words.
  - Real computer: 500 million 64-bit words.
- Address specifies which word.
- If write = 1, input gets copied into chosen word.
- If write = 0, chosen word appears on output.

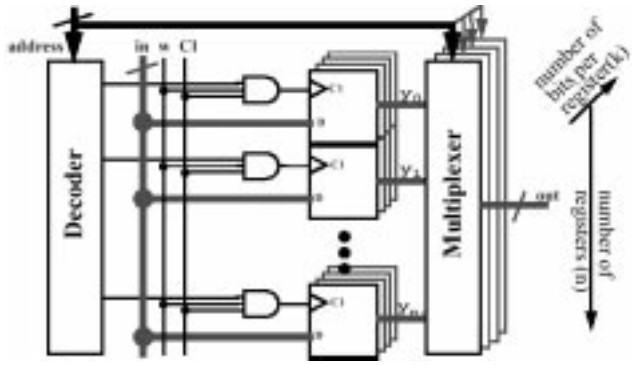


Interface
(8 16-bit words)

Register File (words)

Register file: n registers (words), k bits per register.

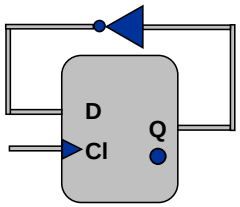
- Single decoder writes k-bit input word to register.
- k multiplexers copy register contents to output.



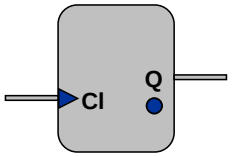
1-Bit Counter

1-bit counter.

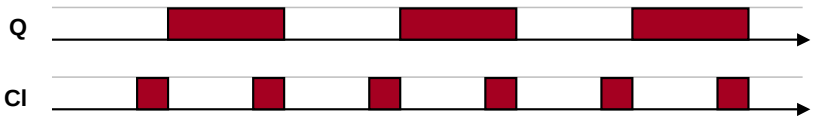
- "Clock" whose cycle is twice as long as input.



Implementation



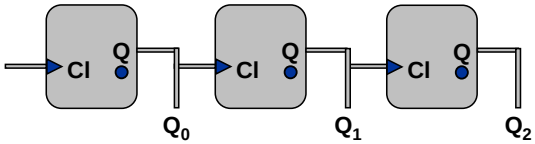
Interface

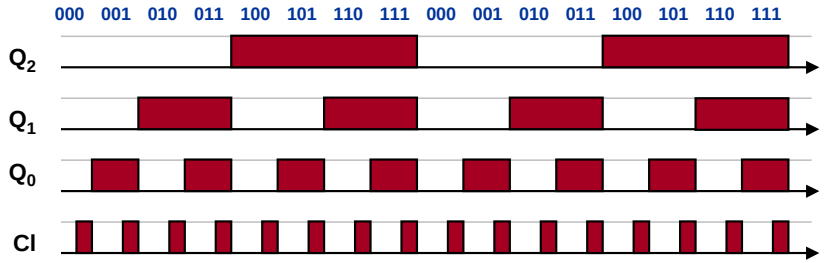


N-Bit Counter

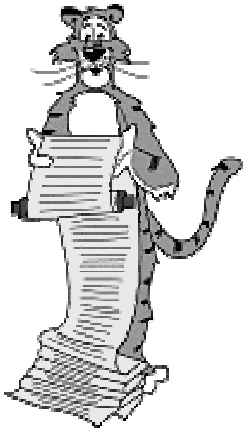
N-bit counter.

- Chain N 1-bit counters together.



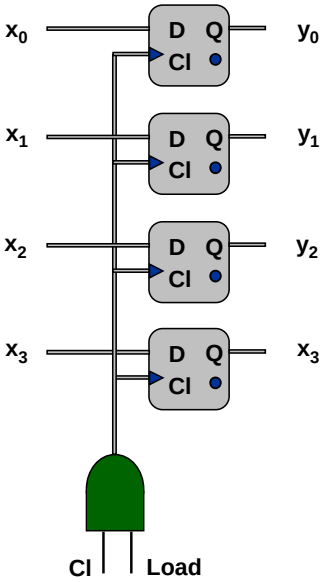


Lecture A4: Extra Slides

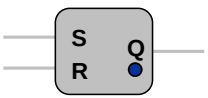


Stand-Alone Register

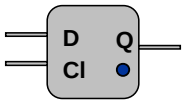
4-bit register.



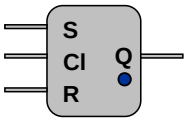
Cheat Sheet



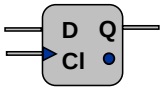
SR flip-flop



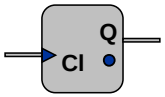
Clocked D flip-flop



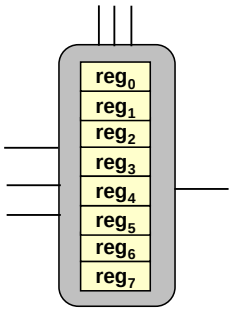
Clocked SR flip-flop



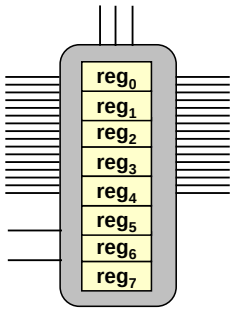
Master-slave flip-flop



1-bit counter



Register File (8 bits)



Register File (8 16-bit words)