Scott C. Karlin

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EDUCATION:

PhD, Computer Science — January 2003
Princeton University, Princeton, NJ
Advisor: Larry Peterson
Thesis: "Embedded Computational Elements in Extensible Routers."

MS, Computer Science — May 1994
Loyola Marymount University, Los Angeles, CA
Coursework in Information Theory, Space Mathematics, Computer Graphics, Real-Time Programming.

BS, Electrical Engineering — June 1986
California Institute of Technology, Pasadena, CA

AWARDS:

Intel Foundation Graduate Fellowship for academic year 1999–2000.
Engineering Council Award for Excellence in Teaching for COS 217, *Introduction to Programming Systems*, fall 1998.

RESEARCH INTERESTS:

My research interests primarily lie near the interface between the hardware and the software in computer systems. This includes operating systems, networking, embedded systems, FPGA-based systems, and hardware design. I also have an active interest in information security and privacy.

RESEARCH EXPERIENCE:

Research Associate — November 2002 – present
Princeton University Computer Science Department, Princeton, NJ
- Researcher for PlanetLab (www.planet-lab.org), a global testbed for developing, deploying, and accessing new planetary-scale network services. Currently investigating resource allocation and management.

Research Assistant — February 1999 – August 2002
Princeton University Computer Science Department, Princeton, NJ — June 1997 – August 1998
- Researcher in the Network Systems Group. Designed and developed key portions of an extensible router using line cards based on Intel IXP1200 network processors and embedded PowerPC processors.

Research Staff — June 1996 – August 1996
Princeton University Computer Science Department, Princeton, NJ
- Researcher for the SHRIMP Project. Designed and supervised the fabrication of the SurfBoard, a custom hardware performance monitor for the SHRIMP system.

Summer Technical Staff / Consultant — June 1998 – September 1999
Sarnoff Corporation, Princeton, NJ
- Research in FPGA based network packet processing. Developed portions of runtime hardware library in VHDL for a C-like language compiler for a hybrid FPGA/processor system.

Project Engineer — August 1986 – March 1995
Data Technologies Division, TRW, Redondo Beach, CA
- Principal Investigator for an R&D project to design systems for processing frequency-agile signals.
- Associate Principal Investigator for an R&D project to develop a parallel processing architecture using the High-Performance Parallel Interface (HIPPI) to connect multiple VME card cages.

RESEARCH EXPERIENCE (continued):

Research Assistant June 1984 – January 1985
Caltech Concurrent Computing Project, California Institute of Technology, Pasadena, CA

- Design and implementation of algorithms for a 64 node concurrent processor. Results presented at the International Conference on Parallel Processing.

TEACHING EXPERIENCE:

Teaching Assistant 1996 – 1998
Princeton University Computer Science Department, Princeton, NJ

- COS 217, Introduction to Programming Systems, fall 1998
- COS 126, General Computer Science, spring 1997
- COS 471, Computer Architecture and Organization, fall 1996

Project Engineer August 1986 – March 1995
Data Technologies Division, TRW, Redondo Beach, CA

- Instructor for the internal *Programming in "C" for Software Engineers* course. The course consisted of Twelve 2 hour classes. Class size ranged between 15 and 40 students per session.

Teaching Assistant September 1983 – June 1986
Electrical Engineering Department, California Institute of Technology, Pasadena, CA

- Teach weekly recitation section, write assignments, grade homework, tutor students, and maintain laboratory. Class covers microprocessor-based systems.

PROFESSIONAL EXPERIENCE:

Manager, Real-Time Data Systems March 1995 – May 1996
Information Management Group, Nicholas Applegate Capital Management, San Diego, CA

- Responsible for real-time data feeds which provide stock prices to the entire firm.

Project Engineer August 1986 – March 1995
Data Technologies Division, TRW, Redondo Beach, CA

- Software engineer for heterogeneous multiprocessor system Designed and implemented a subsystem which used multiple processors to perform bit, frame, and block synchronization as well as error correction on a high-speed data stream in real-time. Developed a portable, real-time kernel, interprocessor communication library, and operating environment which was used throughout the real-time section of the system.
- Hardware designer for the Fast Fourier Transform Processor. This processor performed 16384-point radix-4 FFTs on a continuous data stream of 40 million complex floating point samples per second.
- Proposal team member for six large government contracts.

Member of the Technical Staff June 1986 – August 1986
The Aerospace Corporation, El Segundo, CA

- Installed a commercial hypercubic concurrent processor and instructed employees in its use.

Technical Assistant summer 1982, 1983, 1985
Image Exploitation Department, The Aerospace Corporation, El Segundo, CA part time 1981–82

- Design of tracking algorithms using cellular logic for systolic processing architectures.

PROFESSIONAL SERVICE:

Program Committee member and Webmaster for *OPENARCH 2002*, June 2002.
Program Committee member for *OPENARCH 2003*, April 2003.

COMMUNITY ACTIVITIES:

Community Theatre including several principal acting roles in plays and musicals.
Coach for Little League Baseball and youth soccer.

PAPERS:

S. Karlin, L. Peterson. VERA: An Extensible Router Architecture. *Computer Networks*, 38(3):277–293, February 2002. An earlier version appears in the *Proceedings of the 4th International Conference on Open Architectures and Network Programming (OPENARCH)*, pages 3–14, Anchorage, Alaska, April 2001.

N. Shalaby, L. Peterson, A. Bavier, Y. Gottlieb, S. Karlin, A. Nakao, X. Qie, T. Spalink, M. Wawrzoniak. Extensible Routers for Active Networks. In *Proceedings of the DARPA Active Networks Conference and Exposition*, pages 92–116, San Francisco, California, May 2002.

S. Karlin, L. Peterson. Maximum Packet Rates for Full-Duplex Ethernet. Technical Report TR–645–02, Princeton University, Princeton, New Jersey, February 2002.

T. Spalink, S. Karlin, L. Peterson, Y. Gottlieb. Building a Robust Software-Based Router Using Network Processors. In *Proceedings of the 18th ACM Symposium on Operating Systems Principles (SOSP)*, pages 216–229, Chateau Lake Louise, Banff, Alberta, Canada, October 2001.

X. Qie, A. Bavier, L. Peterson, S. Karlin. Scheduling Computations on a Programmable Router. In *Proceedings of the ACM SIGMETRICS 2001 Conference*, pages 13–24, Cambridge, Massachusetts, June 2001.

T. Spalink, S. Karlin, L. Peterson. Evaluating Network Processors in IP Forwarding. Technical Report TR–626–00, Princeton University, Princeton, New Jersey, November 2000.

L. Peterson, S. Karlin, K. Li. OS Support for General-Purpose Routers. In *Proceedings of the 7th Workshop on Hot Topics in Operating Systems (HotOS–VII)*, pages 38–43, Rio Rico, Arizona, March 1999.

S. Karlin, D. Clark, M. Martonosi, SurfBoard – A Hardware Performance Monitor for SHRIMP. Technical Report TR–596–99, Princeton University, Princeton, New Jersey, March 1999.

M. Martonosi, S. Karlin, C. Liao, D. Clark. Performance Monitoring Infrastructure in Shrimp Multicomputers. *International Journal of Parallel and Distributed Systems and Networks (Invited paper in the special issue on Measurement of Program and System Performance)*, 2(3):126–133, 1999.

E. Felten, S. Karlin, S. Otto. The Traveling Salesman Problem on a Hypercubic, MIMD Computer. In *Proceedings of the 1985 International Conference on Parallel Processing*, pages 6–10, St. Charles, Illinois, August 1985.

E. Felten, S. Karlin, S. Otto. Sorting on a Hypercubic, MIMD Computer. Technical Report HM92B, Caltech Concurrent Computation Project, California Institute of Technology, Pasadena, California, 1985.