

# Guilherme de Lima Ottoni

## Curriculum Vitae

### CONTACT INFORMATION

Intel Corporation  
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### EDUCATION

*Princeton University*, Princeton, NJ, USA

Ph.D. in Computer Science, September 2008

Thesis: “Global Instruction Scheduling for Multi-Threaded Architectures”

Committee: David August, Sharad Malik, Vivek Sarkar, Margaret Martonosi, David Walker

M.A. in Computer Science, GPA 4.0/4.0, April 2005

Advisor: Prof. David I. August

*Universidade Estadual de Campinas (UNICAMP)*, Campinas, SP, Brazil

M.S. in Computer Science, GPA 4.0/4.0, December 2002

Advisor: Prof. Guido Araújo

*Fundação Universidade Federal do Rio Grande (FURG)*, Rio Grande, RS, Brazil

B.S.E. in Computer Engineering, GPA 9.6/10.0 (highest ever), January 2000

*Colégio Técnico Industrial (CTI-FURG)*, Rio Grande, RS, Brazil

Technical High-School in Data Processing, GPA 9.2/10.0 (highest in class), December 1995

### EXPERIENCE

**Research Scientist**, since August 2008

*Intel Corporation*

*Microarchitecture Research Lab*, Santa Clara, CA, USA

Doing research on compiler and microarchitecture techniques to optimize and parallelize applications for modern and future Intel microprocessors.

Manager: Dr. Hong Wang

**Research Assistant**, September 2003 to August 2008

*Liberty Research Group*

*Department of Computer Science, Princeton University*, Princeton, NJ, USA

Worked on a number of projects, but mainly on automatic compiler techniques to extract thread-level parallelism from general-purpose, sequential applications.

**Graduate Research Intern**, June 2006 to September 2006

*Intel Corporation*

*Programming Systems Lab*, Santa Clara, CA, USA

Did research on software redundant multi-threading for error detection and recovery using transactional memory technology. Implemented technique in the Intel Proton x86 production compiler.

Manager: Dr. Youfeng Wu

**Graduate Research Intern**, June 2005 to September 2005

*Intel Corporation*

*Intel Compiler Lab / Microarchitecture Research Lab*, Santa Clara, CA, USA

Did research on automatic compiler techniques to extract task-queuing parallelism. Implemented a prototype in the Intel Proton x86 production compiler, and wrote a patent.

Managers: Dr. Xinmin Tian and Dr. Hong Wang

**Software Engineer**, January 2003 to June 2003

*Motorola, Inc.*

*Eldorado Research Institute*, Campinas, SP, Brazil

Worked on the development of software tools to program cell phones.

**Research Assistant**, March 2000 to December 2002

*Computer Systems Lab*

*Institute of Computing, UNICAMP*, Campinas, SP, Brazil

Did research on compiler optimizations for embedded processors.

**Book Exercise Creator**, January 2002 to September 2002

*Morgan Kaufmann Publishers, Inc.*

Proposed 21 exercises that appear in the book “Engineering a Compiler”, authored by Keith Cooper and Linda Torczon (Rice University).

**Undergraduate Research Assistant**, March 1999 to January 2000

*Robotics Research Lab*

*Department of Physics, FURG*, Rio Grande, RS, Brazil

Did research on techniques for autonomous robot navigation in unknown environments.

## TEACHING

*COS 126 - General Computer Science*

**Preceptor / Teaching Assistant**, Spring 2008, Princeton University

Introductory course in Computer Science, taught by Prof. Robert Sedgewick. I taught precept sessions twice a week, graded programming assignments and exams, and helped preparing exams.

*COS 217 - Introduction to Programming Systems*

**Preceptor / Teaching Assistant**, Fall 2006, Princeton University

Introductory course in C, x86 assembly, and UNIX programming. Taught by Prof. David August. I taught precept sessions twice a week, taught a guest lecture, graded programming assignments and exams, and helped preparing exams.

*COS 320 - Compiling Techniques*

**Teaching Assistant**, Spring 2005, Princeton University

Introductory course in compilation techniques, including the implementation in ML of a full compiler for a simple language. Taught by Prof. David Walker. I helped implementing full solution to the project, and prepared and graded programming assignments.

*Advanced Algorithms and Programming Techniques*

**Lecturer and Organizer**, 2000 to 2003, Brazilian Computer Society

Taught lectures on advanced algorithms for the top-ranked high-school students in the Brazilian Olympiads in Informatics (OBI). Prepared and graded programming assignments and exams to select the Brazilian team for the International Olympiads in Informatics (IOI).

*ACM International Collegiate Programming Contest*

**Coach**, 2002-2003, UNICAMP

Organized a local contest to select the teams representing UNICAMP in the 2002 South American regional contest. Trained the teams for the regional contest, where they received gold and silver

medals. Trained the gold medalist team for the 2003 ACM World Finals, where it ranked 30th worldwide.

*MC 438 - Analysis of Algorithms I*

**Preceptor / Teaching Assistant**, Spring 2000, UNICAMP

Introductory course in the design and analysis of efficient algorithms, taught by Prof. Celia de Mello. I taught precepts, held office hours, and helped prepare homework assignments.

## RECOGNITION

Intel Foundation Ph.D. Fellowship, 2007-2008.

“Wu Prize for Excellence,” awarded by Princeton University’s School of Engineering and Applied Science for upper-year graduated students who have performed at the highest level in courses, research, and teaching, 2007-2008.

Best Paper Award nominee (one among five), for “Automatic Thread Extraction with Decoupled Software Pipelining,” at the 38th ACM/IEEE International Symposium on Microarchitecture, November 2005.

“Best Paper Award” for “Improving Offset Assignment Through Simultaneous Variable Coalescing,” at the 7th International Workshop on Software and Compilers for Embedded Systems, September 2003.

“Departmental Prize for Academic Merit”, awarded by Princeton University’s Department of Computer Science, 2003-2004.

Princeton University Graduate Fellowship, 2003-2004.

Rice University Graduate Fellowship, 2003-2007 (declined).

“Best Master’s Thesis Award” (2nd prize nationwide) from the Brazilian Computer Society, 2003.

CNPq/CAPES Graduate Fellowship, 2000-2002.

Highest GPA (9.6/10.0) in the Computer Engineering undergraduate program at FURG, among all students ever graduated in this program, 2001.

“Programming Excellence Award”, Upsilon Pi Epsilon Honor Society for Computing Sciences, 2001.

World Finalist at the ACM International Collegiate Programming Contest, ranking 29th and 30th worldwide, 2001 and 2003.

Champion at the ACM South American Collegiate Programming Contest, 2000 and 2002.

Champion at the Brazilian Computer Society’s Annual Programming Marathon, 1999, 2000 and 2002.

Champion at the Brazilian Computer Society’s Programming Olympiad through the Internet – Open Division, 1999.

Champion at the 2nd Mathematics Olympiad of Rio Grande – High-School Division, 1994.

## TALKS

### INVITED TALKS

“From Sequential Programs to Concurrent Threads,” presented at *HP Labs*, Palo Alto, USA, April 2008. Host: Jung Ho Ahn.

“From Sequential Programs to Concurrent Threads,” presented at *Microsoft Research*, Redmond, USA, March 2008. Host: James Larus.

“From Sequential Programs to Concurrent Threads,” presented at *AMD Advanced Architecture and Technology Labs*, Bellevue, USA, March 2008. Host: Alan Lee.

“From Sequential Programs to Concurrent Threads,” presented at *Intel Compiler Labs*, Santa Clara, USA, March 2008. Host: Daniel Lavery.

“From Sequential Programs to Concurrent Threads,” presented at *HP Compiler Group*, Cupertino, USA, March 2008. Host: Bhaskar Janakiraman.

“Global Instruction Scheduling for Communication-Exposed Multi-Threaded Architectures,” presented at *IBM T. J. Watson Research Center*, Yorktown Heights, USA, April 2007. Host: Vivek Sarkar.

“Automatic Thread Extraction with Decoupled Software Pipelining,” presented at *Intel Corporation*, Santa Clara, USA, June 2005. Host: Richard Hankins.

#### CONFERENCE TALKS

“Communication Optimizations for Global Multi-Threaded Instruction Scheduling,” presented at *the 13th International Conference on Architectural Support for Programming Languages and Operating Systems*, Seattle, USA, March 2008.

“Global Multi-Threaded Instruction Scheduling,” presented at *the 40th International Symposium on Microarchitecture*, Chicago, USA, December 2007.

“Global Multi-Threaded Instruction Scheduling: Technique and Initial Results,” presented at *the 6th Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology*, San Jose, USA, March 2007.

“Automatic Thread Extraction with Decoupled Software Pipelining,” presented at *the 38th International Symposium on Microarchitecture*, Barcelona, Spain, November 2005.

“A New Approach to Thread Extraction for General-Purpose Programs,” presented at *the 2nd IBM Watson Conference on Interaction between Architecture, Circuits, and Compilers*, Yorktown Heights, USA, September 2005.

“Decoupled Software Pipelining: A Promising Technique to Exploit Thread-Level Parallelism,” presented at *the 4th Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology*, San Jose, USA, March 2005.

“Algorithms for Global Array Reference Allocation,” presented at *the 16th SBC Theses and Dissertations Workshop*, Campinas, Brazil, August 2003.

“Efficient Array Reference Allocation for Loops in Embedded Processors,” presented at *the IEEE Workshop on Embedded System Codesign*, San Jose, USA, September 2002.

“Path Planning for Mobile Robots in Unknown Environments,” presented at *the 13th Brazilian Conference on Automation*, Florianópolis, Brazil, September 2000.

#### PROFESSIONAL ACTIVITIES

##### VOLUNTEER WORK

*ACM International Collegiate Programming Contest, 2004 to present*

Member of the scientific committee responsible for creating the problem set for the Brazilian and South American regional contests.

### *Brazilian Olympiads in Informatics, 2000 to 2003*

Co-organizer, joint with Prof. Ricardo Anido (UNICAMP). Responsible for creating and grading problem sets, and organizing nationwide competitions with thousands of students from high school and middle school. Also coordinated the annual “Advanced Algorithms and Programming” course offered to the top students, and served as a co-leader for the Brazilian teams at the International Olympiads in Informatics.

### REVIEWS

Journals: ACM Transactions on Architecture and Code Optimization, IEEE Micro, IEEE Transactions on Parallel and Distributed Systems, ETRI Journal

Conferences: ASPLOS, PLDI, MICRO, ISCA, CASES, CGO, HPCA, ICCAD, ICCD, INTERACT, ISPASS

### GRANTS

Assisted Professors David August, Scott Mahlke, and Kim Hazelwood with the proposal “Scalable Automatic Thread Extraction of C/C++ Codes for Multicore Systems,” in submission to Semiconductor Research Corporation, November 2007.

Assisted Professors David August, Kim Hazelwood, and Scott Mahlke with the proposal “Revisiting the Sequential Programming Model for Multicore Systems,” in submission to NSF, December 2007.

Assisted Professors Luis Ceze, Mark Oskin, David August, and Susan Eggers with the proposal “A HW/SW Interface Designed for a Parallelizing Compiler,” in submission to NSF, December 2007.

### PUBLICATIONS

#### JOURNAL PUBLICATIONS

- [1] Ram Rangan, Neil Vachharajani, Guilherme Ottoni, and David I. August, “Performance Scalability of Decoupled Software Pipelining,” in *ACM Transactions on Architecture and Code Optimization (TACO)*, August 2008.
- [2] Desiree Ottoni, Guilherme Ottoni, Guido Araujo, and Rainer Leupers, “Offset Assignment Using Simultaneous Variable Coalescing,” in *ACM Transactions on Embedded Computing Systems (TECS)*, November 2006.
- [3] Guilherme Ottoni, Ram Rangan, Adam Stoler, Matthew J. Bridges, and David I. August, “From Sequential Programs to Concurrent Threads,” in *IEEE Computer Architecture Letters (CAL)*, June 2005.
- [4] Guilherme Ottoni and Walter Lages, “Navigation of Mobile Robots in Unknown Environments Using Ultrasound Sonars,” in *SBA Journal of Control and Automation*, November 2003.
- [5] Guilherme Ottoni and Guido Araujo, “Address Register Allocation for Arrays in Loops of Embedded Programs,” in *Microelectronics Journal – Special Issue on IEEE Workshop on Embedded System Code-sign*, November 2003.
- [6] Guido Araujo, Guilherme Ottoni, and Marcelo Cintra, “Global Array Reference Allocation,” in *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, April 2002.

- [1] Easwaran Raman, Guilherme Ottoni, Arun Raman, Matthew Bridges, and David I. August, “Parallel-Stage Decoupled Software Pipelining,” in *Proceedings of the 2008 International Symposium on Code Generation and Optimization (CGO)*, April 2008.
- [2] Guilherme Ottoni and David I. August, “Communication Optimizations for Global Multi-Threaded Instruction Scheduling,” in *Proceedings of the 13th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2008.
- [3] Guilherme Ottoni and David I. August, “Global Multi-Threaded Instruction Scheduling,” in *Proceedings of the 40th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2007.
- [4] Neil Vachharajani, Ram Rangan, Easwaran Raman, Matthew J. Bridges, Guilherme Ottoni, and David I. August, “Speculative Decoupled Software Pipelining,” in *Proceedings of the 16th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2007.
- [5] Ram Rangan, Neil Vachharajani, Adam Stoler, Guilherme Ottoni, David I. August, and George Z. N. Cai, “Support for High-Frequency Streaming in CMPs,” in *Proceedings of the 39th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2006.
- [6] Matthew J. Bridges, Neil Vachharajani, Guilherme Ottoni, and David I. August, “Automatic Instruction Scheduler Retargeting by Reverse-Engineering,” in *Proceedings of the 2006 ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2006.
- [7] Spyridon Triantafyllis, Matthew J. Bridges, Easwaran Raman, Guilherme Ottoni, and David I. August, “A Framework for Unrestricted Whole-Program Optimization,” in *Proceedings of the 2006 ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2006.
- [8] Bolei Guo, Youfeng Wu, Cheng Wang, Matthew J. Bridges, Guilherme Ottoni, Neil Vachharajani, Jonathan Chang, and David I. August, “Selective Runtime Memory Disambiguation in a Dynamic Binary Translator,” in *Proceedings of the 15th International Conference on Compiler Construction (CC)*, March 2006.
- [9] Guilherme Ottoni, Ram Rangan, Adam Stoler, and David I. August, “Automatic Thread Extraction with Decoupled Software Pipelining,” in *Proceedings of the 38th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, November 2005.  
**One of five papers nominated for the Best Paper Award by the Program Committee.**
- [10] Guilherme Ottoni, Ram Rangan, Adam Stoler, and David I. August, “A New Approach to Thread Extraction for General-Purpose Programs,” in *Proceedings of the 2nd Watson Conference on Interaction between Architecture, Circuits, and Compilers (PAC2)*, September 2005.
- [11] Bolei Guo, Matthew J. Bridges, Spyridon Triantafyllis, Guilherme Ottoni, Easwaran Raman, and David I. August, “Practical and Accurate Low-Level Pointer Analysis,” in *Proceedings of the Third International Symposium on Code Generation and Optimization (CGO)*, March 2005.
- [12] Neil Vachharajani, Matthew J. Bridges, Jonathan Chang, Ram Rangan, Guilherme Ottoni, Jason A. Blome, George A. Reis, Manish Vachharajani, and David I. August, “RIFLE: An Architectural Framework for User-Centric Information-Flow Security,” in *Proceedings of the 37th International Symposium on Microarchitecture (MICRO)*, December 2004.
- [13] Guilherme Ottoni, Sandro Rigo, Guido Araujo, Subramanian Rajagopalan, and Sharad Malik, “Optimal Live Range Merge for Address Register Allocation in Embedded Programs,” in *Proceedings of the 10th International Conference on Compiler Construction, LNCS 2027 (CC)*, April 2001.
- [14] Guilherme Ottoni and Walter Lages, “Path Planning for Mobile Robots in Unknown Environments,” in *Proceedings of the 13th Brazilian Automation Conference (CBA)*, September 2000.

## REFEREED WORKSHOP PUBLICATIONS

- [1] Guilherme Ottoni and David I. August, “Global Multi-Threaded Instruction Scheduling: Technique and Initial Results,” in *Proceedings of the Sixth Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC)*, March 2007.
- [2] Guilherme Ottoni, Ram Rangan, Neil Vachharajani, and David I. August, “Decoupled Software Pipelining: A Promising Technique to Exploit Thread-Level Parallelism,” in *Proceedings of the Fourth Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC)*, March 2005.
- [3] Desiree Ottoni, Guilherme Ottoni, Guido Araujo, and Rainer Leupers, “Improving Offset Assignment through Simultaneous Variable Coalescing,” in *Proceedings of the 7th International Workshop on Software and Compilers for Embedded Systems, LNCS 2826 (SCOPES)*, September 2003.  
**Best Paper Award.**
- [4] Guilherme Ottoni and Guido Araujo, “Algorithms for Global Array Reference Allocation in DSPs,” in *Proceedings of the 16th Theses and Dissertations Workshop – Brazilian Computer Society*, August 2003.  
**Best Master’s Thesis Award (2nd Prize Nationwide).**
- [5] Guilherme Ottoni and Guido Araujo, “Efficient Array Reference Allocation for Loops in Embedded Processors,” in *Proceedings of the IEEE Workshop on Embedded System Codesign*, September 2002.

## OTHER PUBLICATIONS

- [1] Guilherme de Lima Ottoni, “Global Instruction Scheduling for Multi-Threaded Architectures,” Ph.D. Thesis, Princeton University, September 2008.
- [2] Guilherme de Lima Ottoni, “Global Address Register Allocation for Array References in DSPs,” Master’s Thesis, Universidade Estadual de Campinas (UNICAMP), December 2002.  
**Best Master’s Thesis Award (2nd Prize Nationwide).**
- [3] Guilherme de Lima Ottoni, “Path Planning for Mobile Robots,” Senior Thesis, Fund. Universidade Federal do Rio Grande (FURG), January 2000.

## PATENTS

- [1] Guilherme Ottoni, Xinmin Tian, Hong Wang, Richard Hankins, Wei Li, and John P. Shen, “Method, System, and Program of a Compiler to Parallelize Source Code,” United States Patent Number 20070234276, Assignee Intel Corporation, October 2007.