# MARCELO ORENES-VERA

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I am Ph.D. candidate in CS at Princeton University, advised by Prof. Margaret Martonosi and Prof. David Wentzlaff. My research interest lies in software-hardware co-designs and how to exploit optimizations at different layers of the computing stack to achieve cumulated improvements in performance and energy efficiency. Since starting my Ph.D., I have been improving power, performance, area, and cost of computing systems that focus on Graph Applications, Sparse Linear Algebra, and HPC, where my work achieves strong scaling up to over a million processing elements.

As Moore's law returns slow down and Dennard Scaling has ended, full-stack optimization is getting more necessary to meet workloads performance at reasonable power. Throughout my education and work experience, I've acquired the skills to research and develop optimizations in computer systems, from transistors up to applications. This holistic view has enabled me to contribute to distinct but complementary domains like formal verification and software programmability of heterogeneous hardware.

During my Ph.D., I've been working on the DARPA-funded DECADES project to demonstrate the promise of a heterogeneous tile-based architecture designed for several emerging workflows in the broad areas of Machine Learning and Graph Analytics. This project led to a chip tapeout where I've contributed at every aspect of the computing stack, ranging from new programming models, applications, OS support, assembly libraries, RTL design and verification, and physical design.

In the publications section, you can find the projects I've led and participated on. I've enjoyed collaborating within and across teams in industry and academia to develop large projects. Proof of this is having successfully contributed to three GPUs at Arm, two academic chip tapeouts, and several research collaborations.

## EDUCATION

**Ph.D. in Computer Science** Expected May 2024
Princeton University, USA

- Advisors: Prof. Margaret Martonosi and Prof. David Wentzlaff
- Dissertation: Navigating Heterogeneity and Scalability in Modern Chip Design

**Master's degree in Computer Science** May 2021
Princeton University, USA

- GPA: 3.95/4.0

**International Exchange, Computer Science** Sept. 2015 - Jan. 2016
University of Hasselt, Belgium

- Projects: MySiri (android app for voice recognition and pattern matching that achieved over 100K downloads at the Google Play Store) and an augmented reality Pong game (involving Microsoft's Surface Table, QR-detected tangibles, voice recognition, light tracking and smartphone controls).

**Bachelor's degree in Computer Science** June 2017
University of Murcia, Spain

- GPA: 9.65/10. Ranked 1st of the class.
- Thesis: An Indoor Location and Guidance System with Automated User Trajectory Analysis.
- Summa Cum Laude.

## HONORS AND AWARDS

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| IEEE MICRO Top Picks honorable mention | 2023 |
| Gold Medal at the ACM/SIGMICRO Student Research Competition (SRC) | Chicago, 2022 |
| COSCON hackathon 4th place graduate team | Princeton, 2021 |
| Best Paper nomination ISPASS | Boston, 2020 |
| 1st prize ARM Norway Microbit hackathon | Trondheim, 2019 |
| Extraordinary Prize for University of Murcia's best students of the year | Murcia, 2017 |
| Computer Science department's Award for Excellence | Murcia, 2017 |
| NASA Space Apps hackathon, Best-concept prize *"Automated Exploration System"* | Murcia, 2017 |
| Government of Spain's Scholarship for bachelor studies | Madrid, 2016 |
| 1st prize Santander's Bank math & problem-solving contest | Murcia, 2015 |
| Highest-score SAT Scholarship from University of Murcia | Murcia, 2013 |

## RESEARCH & INDUSTRY EXPERIENCE

**Princeton University,** Dept. of Computer Science and Engineering August 2019-Present
**Research Assistant**
Advisors: Prof. Margaret Martonosi and Prof. David Wentzlaff

- Developing and testing hardware-software co-design approaches to mitigate the long latency of irregular memory accesses in graph applications and sparse linear algebra kernels.
- Software programmability and OS support of specialized memory access hardware.
- Contributing to the development and verification of a reconfigurable heterogeneous SoC that provides compiler-time specialization based on applications needs, as part of DARPA's Software Defined Hardware (SDH) program.

**AMD Research,** Austin, Texas January 2023-August 2023
**Research and Development, Internship**

- Massively parallelize kernels that traverse sparse data structures and analyze bottlenecks when scaling graph traversal to petabyte-scale graphs.
- Design hardware accelerators for key functionality that is common within these kernels.
- Characterize end-to-end applications that are key for the intelligence community such as knowledge graphs to inform the design of the next generation of AMD's data-center systems.
- Determine the granularity and integration of memory and compute for such systems.

**Cerebras Systems Inc,** Sunnyvale, California May 2021-June 2022
**Application Kernel Engineer, Internship**

- Analyze performance bottlenecks of different mappings of massively parallel applications.
- Use state-of-the-art parallelization and partitioning techniques to automate generation, exploiting hand-written distributed kernels, e.g., FFT (*publication soon*), BFS/SSSP, SPMV, etc.
- Evaluate the performance of different HPC applications on the Cerebras WSE
- Employ and extend state of the art program analysis methods such as the Integer Set Library.

**ARM Ltd,** Trondheim, Norway July 2017-August 2019
**Hardware Engineer**

- Investigation and design of optimizations to the current implementation of several modules within the Texture Mapper of the Mali GPU, specifically Texture Cache and fetch engine.
- Multilevel cache systems development and replacement policies optimizations for improved performance density and bandwidth saving.
- Formal Verification of several modules at unit-level and bug hunting for liveness properties across units. Constrained randomized testing using UVM for the entire Texture Mapper.
- Worked on design and verification across the MALI GPUs G76, G77 and G78 projects.

**Murcia University,** Dept. of Computer Science February 2016-June 2017
**Research Assistant**
Advisor: Prof. Mercedes Valdes-Vela

- Developing a platform for indoor location based on Bluetooth 4.0 LE technology.
- Deploying Android and iOS Apps that based on the location of a visitor in a museum, it provides media content of cultural events near their location.
- Analysis of real museum visitor trajectories using Machine Learning and classifying them in customer profiles using clustering techniques.

**SecondLemon SL,** Murcia, Spain June 2015-September 2015
**Software Engineer,** Internship

- Full-stack analysis and development of iOS and Android apps.
- Development and deployment of backend web services in Java with JSON-REST.

## TEACHING EXPERIENCE

**Teaching Assistant**
COS/ECE 475 "Computer Architecture". Princeton University January – May 2021

- Instructed several lectures about principles of hardware design in Verilog RTL
- Assisted designing the course's curriculum and grading midterm and final exams.
- Prepared and graded four lab deliverables about RTL design of a RISC-V processor core.
- Held weekly office hours with the students to assist with problem sets and labs.
- Proposed and supervised the course's final research projects.

**Research co-supervision for Undergraduate Students**
Dept. Computer Science (CS) and Dept. Electrical and Computer Engineering (ECE), Princeton University
CS Senior Thesis (Hyunsung Hun) Sept. 2021 – May 2022

- Leveraging hardware Formal Verification to automatically detect microarchitectural covert channels in time-shared hardware. The work from this thesis led to a top-tier publication.

ECE Junior Independent Work (Varun Deb) Jan. 2022 – May 2022

- Techniques for enhanced performance analysis in large manycore architectures.

ECE Senior Thesis (Markos Markakis) Sept. 2019 – May 2020

- Formal Verification of a memory-fetch engine within the context of a heterogeneous SoC that we eventually taped-out. This thesis got the SEAS Calvin Dodd MacCracken Award.

**Residential College's Graduate Student Mentor**
New College West, Princeton University Sept. 2022 – May 2024
First College, Princeton University Sept. 2021 – May 2022

- Organized and led professional development activities for upper-class undergraduate students.
- Advised Senior students during the yearly winter thesis bootcamp.
- Mentored >30 first-year students per year (1-1 and group mentoring for academic and career goals)

## CONFERENCE PAPERS

**Marcelo Orenes-Vera**, Hyunsung Yun, Nils Wistoff, Luca Benini, Gernot Heiser, David Wentzlaff and Margaret Martonosi. "AutoCC: Automatic discovery of Covert Channels in Time-Shared Hardware." To appear in Proc. of the 56th International Symposium on Microarchitecture (MICRO). IEEE/ACM 2023.

- Open source formal verification methodology that exhaustively examines RTL to find covert channels where machine state left by a process after a context switch creates an observable execution difference.

**Marcelo Orenes-Vera**, Esin Tureci, David Wentzlaff, and Margaret Martonosi. "Massive, Data-Centric Parallelism in the Chiplet Era." Submitted for publication 2023. Early access.

**Marcelo Orenes-Vera**, Ilya Sharapov, Robert Schreiber, Mathias Jacquelin, Philippe Vandermersch and Sharan Chetlur. "Wafer-Scale Fast Fourier Transforms." In Proc. of the 37th International Conference in Supercomputing (ICS). ACM 2023

**Marcelo Orenes-Vera**, Esin Tureci, David Wentzlaff, and Margaret Martonosi. "Dalorex: A Data-Local Program Execution and Architecture for Memory-bound Applications." In Proc. of the 29th International Symposium in High Performance Computer Architecture (HPCA). IEEE 2023.

Tianrui Wei, Nazerke Turteyeva, **Marcelo Orenes-Vera**, Omkar Lonkar, Jonathan Balkind "Cohort: Software-Oriented Acceleration for Heterogeneous SoCs." In Proc. of 28th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), ACM 2023.

- Open-source SoC generator including the Cohort engine inside OpenPiton. Cohort connects producers and consumers in software with accelerators with minimal application changes.

Fei Gao, Ting-Jung Chang, Ang Li, **Marcelo Orenes-Vera**, Davide Giri, Paul Jackson, August Ning, Georgios Tziantzioulis, Joseph Zuckerman, Jinzheng Tu, Kaifeng Xu, Grigory Chirkov, Gabriele Tombesi, Jonathan Balkind, Margaret Martonosi, Luca Carloni, David Wentzlaff "DECADES: A 67mm2, 1.46TOPS, 55 Giga Cache-Coherent 64-bit RISC-V Instructions per second, Heterogeneous Manycore SoC with 109 Tiles including Accelerators, Intelligent Storage, and eFPGA in 12nm FinFET." In Proc. of the Custom Integrated Circuits Conference (CICC), IEEE 2023.

Ting-Jung Chang, Ang Li, Fei Gao, Tuan Ta, Georgios Tziantzioulis, Yanghui Ou, Moyang Wang, Jinzheng Tu, Kaifeng Xu, Paul J. Jackson, August Ning, Grigory Chirkov, **Marcelo Orenes-Vera**, Shady Agwa, Xiaoyu Yan, Eric Tang, Jonathan Balkind, Christopher Batten, David Wentzlaff "CIFER: A 12nm, 16mm2, 22-Core SoC with a 1541 LUT6/mm2, 1.92 MOPS/LUT, Fully Synthesizable, Cache-Coherent, Embedded FPGA". In Proc. of the Custom Integrated Circuits Conference (CICC), IEEE 2023.

**Marcelo Orenes-Vera**, Aninda Manocha, Jonathan Balkind, Fei Gao, Juan Luis Aragón, David Wentzlaff, and Margaret Martonosi. "Tiny but Mighty: Designing and Realizing Scalable Latency Tolerance for Manycore SoCs." In Proc. of the 49th International Symposium of Computer Architecture (ISCA). ACM 2022. **IEEE Micro Top Picks Honorable Mention.**

- Open-source RTL IP block integrated via the NoC that serves a specialized memory-fetch engine to provide memory-latency for memory-bound applications by offloading indirect memory accesses.

**Marcelo Orenes-Vera**, Aninda Manocha, David Wentzlaff, and Margaret Martonosi. "AutoSVA: Democratizing Formal Verification of RTL Module Interactions." In Proc. of the 58th International Design and Automation Conference (DAC). ACM/IEEE 2021.

- Open-source generator of Formal Verification testbenches. Starred by users from 20+ universities and companies, including AMD, Qualcomm, Axelera AI, Texas A&M, UCB, ETH, HKUST, KAIST, etc.

Opeoluwa Matthews, Aninda Manocha, Davide Giri, **Marcelo Orenes-Vera**, Esin Tureci, Tyler Sorensen, Tae Jun Ham, Juan L. Aragón, Luca P. Carloni, and Margaret Martonosi. "MosaicSim: A Lightweight, Modular Simulator for Heterogeneous Systems." In Proc. of the International Symposium on Performance Analysis of Systems and Software (ISPASS). IEEE 2020. **Best Paper nomination.**

- Open-source simulator for combinations of general-purpose cores and hardware accelerators.

Tyler Sorensen, Aninda Manocha, Esin Tureci, **Marcelo Orenes-Vera**, Juan L. Aragón and Margaret Martonosi, "A Simulator and Compiler Framework for Agile Hardware-Software Co-design Evaluation." International Conference on Computer Aided Design (ICCAD). ACM/IEEE 2020.

## JOURNAL PAPERS

Ang Li, Ting-Jung Chang, Fei Gao, Tuan Ta, Georgios Tziantzioulis, Yanghui Ou, Moyang Wang, Jinzheng Tu, Kaifeng Xu, Paul J. Jackson, August Ning, Grigory Chirkov, **Marcelo Orenes-Vera**, Shady Agwa, Xiaoyu Yan, Eric Tang, Jonathan Balkind, Christopher Batten, David Wentzlaff
"CIFER: A Cache-Coherent 12nm 16mm2 SoC With Four 64-Bit RISC-V Application Cores, 18 32-Bit RISC-V Compute Cores, and a 1541 LUT6/mm2 Synthesizable eFPGA". Solid-State Circuit Letters. IEEE 2023.

**Marcelo Orenes-Vera**, Fernando Terroso, Mercedes Valdes-Vela, "RECITE: A Framework for User Trajectory Analysis in Cultural Sites." Journal of Ambient Intelligence (JAISE). 2021.

- Open-source user mobile applications and server for user trajectory ML analysis.

## SELECTED TALKS

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| Invited Talk Seminar University of Toronto | July 2023 |
| Paper presentation at the 37th ICS in Florida | June 2023 |
| Invited Talk at Barcelona Supercomputing Center | June 2023 |
| Paper presentation at the 29th HPCA in Montreal, CA | February 2023 |
| Invited Talk at AMD Research | January 2023 |
| Presentation at the Student Research Competition (55thMICRO, Chicago) | October 2022 |
| Paper presentation at the 49th ISCA in NYC | June 2022 |
| Presentation at the 1st Open-Source CompArch Research workshop (NYC) | June 2022 |
| Presentation at 2022 Princeton Research Day | May 2022 |
| Presentation at the YArch workshop (co-located 27thASPLOS, Switzerland) | March 2022 |
| Paper presentation at the 58th DAC, San Francisco | December 2021 |
| Invited Talk at TÜ Dortmund, Germany | November 2021 |
| Presentation at 2021 Princeton Research Day | May 2021 |

## PATENTS

Antonio Garcia-Guirado, **Marcelo Orenes-Vera,** "Data Processing Systems", US11169806B1

## SKILLS

***Algorithms:*** Graph Analytics, Sparse Linear Algebra, FFTs, and other HPC workloads.
***High-level programming languages:*** C/C++/C#, Python, Java/Android, iOS/Obj-C, Bash and Web Dev.
***Low-level and parallel programming languages:*** OpenMP, MPI, CUDA, MIPS and RISC-V Assembly.
***Hardware design and verification:*** Verilog, SystemVerilog Assertions (SVA), UVM, Gate-level simulation.
***EDA Tools:*** Formal Verif. with JasperGold and SymbiYosys, VCS, Verilator, GTKWave, Xcelium, Simvision.
***Other knowledge*:** UNIX, 3D Graphics pipeline, WebGL, SQL.

## COURSEWORK

Advanced **Computer Architecture** · Digital Systems · Automated Reasoning about Software · Computer Networks · Computer Science for Technology Policy · **Systems and Machine Learning** · Fundamentals of Machine Learning · Multimedia Compression · Algorithms and Data Structures · HCI · Microelectronic Devices · Operating Systems · Programming Languages · **Object-oriented Programming** · Linear Algebra · Discrete Mathematics ·Distributed Systems · Formal Languages · Compilers · Entrepreneurship · Software Development · Software Architecture · **Software Quality** · Mobile applications for Android and iOS

## SERVICE

- Mentor first-year graduate students Princeton's ECE 2023-2024
- Graduate student mentor at Princeton University's New College West 2022-2024
- Meet-a-senior student mentoring during ISCA 2023.
- Meet-a-senior student mentoring during ASPLOS 2023
- Princeton University's Buddy program for incoming graduate students 2021-2023
- Graduate student mentor at Princeton University's First College 2021-2022
- Sports committee chair ARM Norway 2018-2019
- Social committee chair ARM Norway 2017-2018
- ARM's liaison with NTNU's ADA program to encourage high schoolers to pursue STEM.
- Volunteer at the Exchange Student Network (ESN) of Murcia during 2016-2017
- University of Murcia's Buddy program for exchange students 2016-2017

## LANGUAGES

**Spanish** (native), **English** (proficient), **Norwegian, Italian, Portuguese** (conversational)
**German/French** (intermediate)

## REFERENCES

Available upon request, from Margaret Martonosi (**Princeton University** professor), David Wentzlaff (**Princeton University** professor), Juan Luis Aragón (**University of Murcia** professor), Antonio Garcia Guirado (**Meta**), Carmelo Giliberto (**ARM**), Robert Schreiber (**Cerebras Systems**), Valerie Chen (**AMD Research**), Georgios Tziantzioulis (**AMD Research**).