

David I. August

Curriculum Vitae

CONTACT INFORMATION

Department of Computer Science
Princeton University
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Princeton, NJ 08540

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<http://www.cs.princeton.edu/~august>

EDUCATION

University of Illinois at Urbana-Champaign

Ph.D. in Electrical and Computer Engineering, May 2000

M.S. in Electrical and Computer Engineering, May 1996

Thesis: Systematic Compilation for Predicated Execution, Advisor: Wen-mei W. Hwu

Rensselaer Polytechnic Institute, Troy, NY

B.S. in Electrical Engineering, Summa Cum Laude (1/1249), May 1993

EXPERIENCE

Associate Professor, July 2006 to Present; **Assistant Professor**, February 2000 to June 2006; **Lecturer**, August 1999 to January 2000

Department of Computer Science, Princeton University, Princeton, NJ

Consultant, August 1998-Present

Intel Corporation, Lucent Technologies, Internection, Parakinetix

Research Intern, May to September 1996, November 1996

Intel Corporation, Santa Clara, CA

Research Intern, May to August 1995

Hewlett Packard Laboratories, Santa Clara, CA

Architecture Validation Engineer, May to August 1994

Intel Corporation, Hillsboro, OR

RECOGNITION

- Nomination of “Fault-tolerant Typed Assembly Language” as a Communications of the ACM (CACM) Research Highlight, September 2008.
- Selection of “Revisiting the Sequential Programming Model for Multi-Core” for IEEE Micro’s “Top Picks” special issue for papers “most relevant to industry and significant in contribution to the field of computer architecture” in 2007.
- Best Paper Award for “Fault-tolerant Typed Assembly Language” at the 2007 ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), June 2007.
- Selection of “Automatic Instruction-Level Software-Only Recovery Methods” for IEEE Micro’s “Top Picks” special issue for papers “most relevant to industry and significant in contribution to the field of computer architecture” in 2006.
- Selection of “Automatic Instruction-Level Software-Only Recovery Methods” for the William C. Carter Award at the International Conference on Dependable Systems and Networks, June 2006.
- Best Paper Award for “SWIFT: Software Implemented Fault Tolerance” at the Third Annual ACM/IEEE International Symposium on Code Generation and Optimization (CGO), March 2005.
- Emerson Electric Company E. Lawrence Keyes ’51 Faculty Advancement Award, June 2003.
- Dean’s letter of recognition for teaching, Spring 2003.
- Best Paper Award for “Compiler Optimization-Space Exploration” at the First Annual ACM/IEEE International Symposium on Code Generation and Optimization (CGO), March 2003.
- Best Student Paper Award for “Microarchitectural Exploration with Liberty” at the 35th Annual ACM/IEEE International Symposium on Microarchitecture (MICRO), November 2002.

- National Science Foundation Faculty Early Career Development Award (CAREER), 2002.
- Invited presentation at University of Virginia, *Top Gun Lecture Series* recognizing “faculty on a trajectory to be research leaders of the coming decades,” December 2001.
- IBM Faculty Partnership Award, 2001-2002.
- Princeton University Research Board Award, 2001-2002.
- One of five featured by *The Chronicle of Higher Education* in its annual list of “New Ph.D.’s to Watch,” September 1999.
- Selection of “A Framework for Balancing Control Flow and Predication” by the program committee for inclusion in special issue of *The International Journal of Parallel Processing* composed of “outstanding papers” from the 30th Annual ACM/IEEE International Symposium on Microarchitecture (MICRO), 1999.
- Intel Foundation Graduate Fellowship, 1996-1997.
- Department of Defense, Office of Naval Research Graduate Fellowship, 1993-1996.
- University of Illinois Henry O. Koehler Graduate Fellowship, 1993-1994.

PROFESSIONAL ACTIVITIES

PROGRAM CHAIR

- The 42nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO) (with José Martínez, Cornell), 2009.
- The Fifth Annual International Symposium on Code Generation and Optimization (CGO) (with Chris J. Newburn, Intel), 2007.
- The IEEE International Conference on Computer Design (ICCD) - Computer Systems Design and Applications Track (with Mark Charney, Intel), 2003.
- The IEEE International Conference on Computer Design (ICCD) - Computer Systems Design and Applications Track (with Mark Charney, Intel), 2002.

EDITING

- Associate Editor, ACM Transactions on Architecture and Code Optimization, January 2006 - present.
- Guest Editor, Computer Languages, Systems and Structures special issue on “Programming Language and Compiler Support for Secure and Reliable Computing,” April 2006.

TECHNICAL PROGRAM COMMITTEES

- The First Workshop on Accelerators for High-performance Architectures (WAHA), 2009
- The Fifth IEEE International Symposium on Workload Characterization (IISWC), 2009.
- The ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), 2008.
- IEEE MICRO Top-Picks in Computer Architecture, 2007.
- The Sixth Annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD), 2007.
- The ACM International Conference on Computing Frontiers (CF), 2007.
- The 34th Annual IEEE/ACM International Symposium on Computer Architecture (ISCA), 2007.
- The 39th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), 2006.
- The International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), 2006.
- The Workshop on Introspective Architectures (WISA), 2006.
- The 15th International Conference on Parallel Architectures and Compilation Techniques (PACT), 2006.
- The Second Workshop on Modeling, Benchmarking and Simulation (MoBS), 2006.
- The 10th Workshop on Interaction between Compilers and Computer Architectures (INTERACT), 2006.
- The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2006.
- The 32nd Annual IEEE/ACM International Symposium on Computer Architecture (ISCA), 2005.
- The Workshop on Modeling, Benchmarking and Simulation (MoBS), 2005.
- The IEEE/ACM International Conference on Computer Aided Design (ICCAD), 2005.
- The International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), 2005.
- The Third Annual International Symposium on Code Generation and Optimization (CGO), 2005.
- The International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), 2004.

- The IEEE International Conference on Computer Design (ICCD) - Computer Systems Design and Applications Track, 2004.
- The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2004.
- The Second Annual International Symposium on Code Generation and Optimization (CGO), 2004.
- The 30th Annual IEEE/ACM International Symposium on Computer Architecture (ISCA), 2003.
- The First Annual International Symposium on Code Generation and Optimization (CGO), 2003.
- The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2003.
- The 35th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), 2002.
- The ACM Workshop on Languages, Compilers, and Tools for Embedded Systems (LCTES), 2002.
- The ACM International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS), 2002.
- The 6th Workshop on Interaction between Compilers and Computer Architectures (INTERACT), 2002.
- The First Annual Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC), 2001.
- The ACM Workshop on Languages, Compilers, and Tools for Embedded Systems (LCTES), 2001.
- The IEEE International Conference on Computer Design (ICCD), 2001.
- The 7th International IEEE Symposium on High-Performance Computer Architecture (HPCA), 2000.
- The IEEE International Conference on Computer Design (ICCD), 2000.

CONFERENCE ORGANIZING AND STEERING COMMITTEES

- Steering Committee, The International Symposium on Code Generation and Optimization (CGO), 2007-2010.
- General Chair, The Fourth Annual International Symposium on Code Generation and Optimization (CGO), 2006.
- Publications Chair, The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2003.
- Finance Chair, The Second Annual International Symposium on Code Generation and Optimization (CGO), 2003
- General Chair, The Second Annual Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC), 2002.

TECHNICAL PANELS

- Panelist, “Freedom from the Tyranny of Parallel Programming,” Workshop on Deterministic Multiprocessing and Parallel Programming (WoDet), November 2009.
- Panelist, “Programming for Multi-core Processors (OR NOT?)” Second Workshop on Computer Architecture Research Directions (CARD) held in conjunction with International Symposium on Computer Architecture (ISCA), June 2009.
- Panelist, “Are New Programming Languages Needed to Exploit Manycore Architectures?” Microsoft Research Faculty Summit, July 2007.
- Panelist, “Programming Languages/Models and Compiler Technologies,” Manycore Computing Workshop held in conjunction with the International Conference on Supercomputing (ICS), June 2007.
- Panelist, “Are New Languages Necessary for Multicore,” The Fifth International Symposium on Code Generation and Optimization (CGO), March 2007.
- Panelist, “Directions in Multi-Core Research,” Microsoft Corporation, Redmond, WA, January 2007.
- Panelist, “What should architects know about compilers and systems software?” The Computing Research Association’s Committee on the Status of Women (CRA-W) and the Coalition to Diversify Computing (CDC) Computer Architecture Summer School, 2006.
- Panelist, “Design Methodologies for Future Processor Chips,” The Second Workshop on Modeling, Benchmarking and Simulation held in conjunction with the 33rd International Symposium on Computer Architecture (ISCA), 2006.
- Panelist, “Simulation Methodology,” Third Annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD) held in conjunction with International Symposium on Computer Architecture (ISCA), 2004.
- Panelist, “Emerging Issues with Simulation Technology” NSF-Sponsored Workshop, Austin, TX, December 2001.

FUNDING PANELS

- National Science Foundation Computing Systems Research Panel (CSR)
- National Science Foundation Computer Systems Architecture Panel (CSA)
- National Science Foundation Medium Information Technology Research Panel (ITR)
- National Science Foundation Next Generation Software Panel (NGS)

TUTORIALS

- “Fault Tolerant Computing,” Summer School on Language-Based Techniques for Integrating with the External World, July 2007.
- “Structural Simulation,” presented at the HiPEAC Compilation and Architecture Summer School in L’Aquila, Italy, June 2005.
- “Using The Liberty Simulation Environment with emphasis on validated OS-level simulation,” presented at the 11th International Conference on Architectural Support for Programming Languages and Operating Systems in Boston, MA, October 2004.
- “The Liberty Simulation Environment, Version 1.0,” presented at the 36th International Symposium on Microarchitecture in San Diego, CA, December 2003.
- “Architectural Exploration with Liberty,” presented at the International Symposium on Microarchitecture in Austin, TX, December 2001.
- “Future Technologies and Markets for Programmable Platform-Based Design,” presented at IP/SoC 2001 in Santa Clara, CA, March 2001.

INVITED TALKS

- Keynote: “Parallelism for Multicore,” presented at the 2009 Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures held in conjunction with 36th International Symposium on Computer Architecture, June, 2009.
- “Parallelism for Multicore,” presented at the New Jersey Programming Languages Seminar and Princeton Computer Architecture Research Day, March, 2009.
- “Addressing the Multicore Problem,” presented at the Princeton Innovation Forum, March, 2009.
- “Automatic Thread Extraction from Sequential Programs,” presented at Indian Institute of Science, March, 2008.
- “The Multicore Challenge,” DARPA Information Processing Technology Office Futures Panel, December 2007.
- “Automatic Thread Extraction from Sequential Programs,” presented at Microsoft Research Faculty Summit, 2007.
- “Liberating Threads from Sequential Programs,” presented at Purdue University, November 2006.
- “The Jericho Project,” presented at the Workshop on Design, Architecture and Simulation of Chip Multi-Processors, November 2005.
- “Liberating Threads from Sequential Programs,” presented at Intel Microprocessor Laboratories, Hewlett-Packard Laboratories, Sun Microsystems Research Laboratories, INRIA Futurs, Cornell University, Carnegie Mellon University, and Massachusetts Institute of Technology, March-April 2005.
- “Liberating Threads from Sequential Programs,” presented at the New Jersey Programming Languages Seminar, February 2005.
- “Liberty Compiler Research,” presented at IBM T. J. Watson Research Center, April 2004.
- “Liberty Research,” presented at Infineon Corporation and Aachen University, February 2004.
- “Architectural Exploration with Liberty,” presented at the Intel High-Level Design Research Forum, November 2002.
- “Optimization-Space Exploration,” presented at Intel Microprocessor Research Laboratories, Hewlett-Packard Laboratories, and Sun Microsystems Research Laboratories, August 2002.
- “Architectural Exploration with Liberty,” presented at IBM T. J. Watson Research Center, July 2002.
- “Liberty Compiler and Architecture Research,” presented at University of Texas at Austin, April 2002.
- “Architectural Exploration with Liberty,” presented at University of Virginia, *Top Gun Lecture Series* recognizing “faculty on a trajectory to be research leaders of the coming decades,” December 2001.
- “Architectural Exploration with Liberty,” presented at Intel Microprocessor Laboratories, Hewlett-Packard Laboratories, and Sun Microsystems Research Laboratories, May 2001.

- “Architectural Exploration with Liberty,” presented at University of Toronto, Distinguished Lecture Series, May 2001.
- “Systematic Compilation for Predicated Execution,” presented at IBM Tokyo Research Laboratories, Rice University, and University of Illinois at Urbana/Champaign, January-August 2000.
- “Systematic Program Decision Logic Optimization Using Predication,” presented at Intel Microprocessor Research Laboratories, April 1999.
- “Enabling Compiler Technology for Predication,” presented at The Swiss Federal Institute of Technology of Lausanne (École Polytechnique Fédérale de Lausanne), February 1999.
- “Enabling Compiler Technology for Predication,” presented at Compaq Corporation, November 1998.
- “A Global Predication Compilation Framework,” presented at Microsoft Research, November 1998.
- “Predicated Microprocessor Architectures and Their Enabling Compiler Technology,” presented at Silicon Graphics, February 1998.
- “Next Generation Predication Support in the IMPACT Compiler,” presented at The Intel Foundation Fellowship Forum, November 1996.
- “Predicated Execution Architectures: New Research Results and Directions,” presented at The Intel Microprocessor Research Forum, October 1995.

GRANTS

- “AESOP: Adaptive Environment for Supercompiling with Optimized Parallelism,” United States Department of Defense (DOD), Defense Advanced Research Projects Agency (DARPA), Architecture-Aware Compiler Environment (AACE) Program, \$11,572,332, 2009 to 2013. (PI with 4 others)
- “Implicitly Parallel Programming with Dynamic Execution,” LG Electronics, \$40,000, November 2009.
- “Hierarchical Latency and Throughput Optimization of Parallel Applications,” Google Research Award, \$50,000, November 2009.
- “Revisiting the Sequential Programming Model for Multicore Systems,” National Science Foundation, Computing Processes and Artifacts (CPA), \$150,000, September 2008 to August 2009. (PI with Hazelwood and Mahlke)
- “Automatically Parallelizing Legacy Binary Code for Multi-Core Architectures via Extraction of Self-Similarity,” DARPA/IPTO, \$300,000, Sep2008 to August 2009. (PI with Locasto, Sethumadhavan, and Stolfo)
- “Liberating Threads from Sequential Programs,” Gigascale Silicon Research Center, \$357,000, September 2006 to August 2009. (Sole PI)
- “Well-typed Trustworthy Computing in the Presence of Transient Faults,” National Science Foundation, CyberTrust Program, \$1,100,000, September 2006 to June 2010. (Co-PI with Walker, Appel, Clark, and Martonosi)
- “Software-Modulated Fault Tolerance,” National Science Foundation, Computer Systems Research (CSR) Program, \$320,000, July 2006 to June 2009. (Sole PI)
- “A Viable Approach to Compiling Sequential Codes for CMPs,” Microsoft Corporation, \$50,000, April 2006.
- “Flow-Based Computer Systems Support for Synergistic Hardware-Software Management of Embedded Systems,” National Science Foundation, Computer Systems Research (CSR) Program, \$500,000, September 2005 to August 2009. (Co-PI with Li, Martonosi, and Pe)
- “User-centric Information Flow Security,” Intel Corporation, \$120,000, August 2005 to July 2008.
- “Threading the CMP Needle with Fibers and Frays,” The Microelectronics Advanced Research Corporation (MARCO), \$122,500, April 2005 to August 2006. (Sole PI)
- “International Modular Simulation Research,” Direction des Relations Européennes et Internationales (DREI), Programme INRIA “Equipes Associées”, €60,000, January 2005 to December 2007. (Co-PI)
- “A Structural and Composable Framework for MP Systems,” Intel Corporation, \$135,000, September 2003.
- “Collaborative Research – Structural and Composable Performance Simulation of Complex Systems,” National Science Foundation, Next Generation Software (NGS) Program, \$1,101,503, September 2003 to August 2006. (PI with Malik, Pai, and Peh)
- Emerson Electric Co. E. Lawrence Keyes '51 Award, \$30,000, June 2003.
- Xilinx Equipment Grant, \$46,300, June 2003.
- “The Mapping Problem,” Infineon Corporation, \$100,000, November 2003.
- “Optimization-Space Exploration,” Intel Corporation, \$53,000, March 2002.

- “Systematic Design-Space Exploration,” National Science Foundation, Faculty Early Career Development Award (CAREER), \$357,130, January 2002 to December 2006. (Sole PI)
- “EPIC Compiler and Architecture Research,” Hewlett-Packard and Intel Corporation Itanium Processor Family Equipment Grant, \$64,960, November 2001. (Coordinated university wide grant of \$242,157.)
- “Analysis Tools for Network Processors,” IBM Corporation, \$30,000, June 2001.
- “Memory Shape and Flow Determination,” Intel Corporation, \$53,000, March 2001.
- “Modern Embedded Systems: Compilers, Architectures, and Languages (MESCAL),” Gigascale Silicon Research Center, \$350,000, January 2001 to December 2003. (Sole PI)
- “Collaborative Research – Ascertaining Runtime Branch Characteristics through Algebraic Analysis of Programs,” National Science Foundation, Information Technology Research (ITR) Program, \$310,000, September 2000 to August 2002. (PI with Clark and Skadron)

UNIVERSITY SERVICE

- Member of Computer Science Department’s Diversity Task Force
- Associate Chair, Computer Science Department, 2007-2008
- University Committee on Examinations and Standing, 2006-2007
- University Committee on Committees, 2002-2005
- Mathey College Faculty Fellow
- Class of 2004, 2005, 2006, 2007, 2008, and 2009 Freshman Advising
- Computer Science Class of 2004 BSE Advising
- School of Engineering and Applied Science *Ad Hoc* Committee on the Computing Requirement
- Co-leader School of Engineering and Applied Science Strategic Planning Executive Committee for Focus on the Faculty.

TEACHING

- COS-126: Introduction to Computer Science (Dean’s letter of recognition for teaching)
- COS-217: Introduction to Programming Systems
- COS-320: Compiler Implementation
- COS-471A, COS-471B/ELE-375: Introduction to Computer Architecture
- COS-598: Feedback-Directed Optimization
- COS-598: Computer Architecture Research Infrastructure Development
- COS-598: Synergistic Hardware-Compiler Architecture Design
- COS-598: Topics in Compiler Construction

STUDENTS

CURRENT DOCTORAL STUDENTS

Thomas Jablin (year 4), Arun Raman (year 4), Yun Zhang (year 4), Prakash Prabhu (year 3), Jialu Huang (year 3), Hanjun Kim (year 3), Jack Tzu-Han Hung (year 3), Nick Johnson (year 2), Alexander Wauck (year 1)

COMPLETED DEGREES

Easwaran Raman

Ph.D. Thesis: Parallelization Techniques with Improved Dependence Handling

First Position: Google

Thomas Mason

Master of Engineering Degree

First Position: Johns Hopkins University Applied Physics Laboratory

Matthew Bridges

Ph.D. Thesis: The VELOCITY Compiler: Extracting Efficient Multicore Execution from Legacy Sequential Codes

First Position: Google

Bolei Guo

Ph.D. Thesis: Shape Analysis with Inductive Recursion Synthesis

First Position: JPMorgan

Neil Vachharajani

Ph.D. Thesis: Intelligent Speculation for Pipelined Multithreading

First Position: Google

Guilherme Ottoni

Ph.D. Thesis: Global Instruction Scheduling for Multi-Threaded Architectures

First Position: Intel Research

George A. Reis

Ph.D. Thesis: Global Instruction Scheduling for Multi-Threaded Architectures

First Position: Google

Ram Rangan

Ph.D. Thesis: Pipelined Multithreading Transformations and Support Mechanisms

First Position: IBM Austin Research Laboratory

Spyridon Triantafyllis

Ph.D. Thesis: Eliminating Conventional Restrictions on Compiler Optimization

First Position: D. E. Shaw

David A. Penry

Ph.D. Thesis: Microarchitecture Modeling for Design-space Exploration

First Position: Assistant Professor at Brigham Young University

Manish Vachharajani, co-advised with Sharad Malik

Ph.D. Thesis: Microarchitecture Modeling for Design-space Exploration

First Position: Assistant Professor at University of Colorado, Boulder

Jason Blome

Master of Engineering Degree

First Position: Ph.D. candidate at University of Michigan, Ann Arbor

PUBLICATIONS

BOOK CHAPTERS

- [1] Neil Vachharajani and David I. August, "Speculation," in *Encyclopedia of Computer Science and Engineering* edited by Benjamin W. Wah, John Wiley Sons, Inc., January 2009. (ISBN: 9780471383932)
- [2] Easwaran Raman and David I. August, "Optimizations for the Memory Hierarchy," in *Compiler Design Handbook* edited by Y. N. Srikant, CRC Press, December 2007.
- [3] David I. August, "Branch Predication," in *Speculative Execution in High Performance Computer Architectures* edited by D. Kaeli and P.-C. Yew, CRC Press, April 2005. (ISBN: 1584884479)

REFEREED JOURNAL PUBLICATIONS

- [4] Ram Rangan, Neil Vachharajani, Guilherme Ottoni, and David I. August, "Performance Scalability of Decoupled Software Pipelining," in *ACM Transactions on Architecture and Code Optimization (TACO)*, August 2008.
- [5] Matthew J. Bridges, Neil Vachharajani, Yun Zhang, Thomas Jablin, and David I. August, "Revisiting the Sequential Programming Model for the Multicore Era," in *IEEE Micro*, January 2008.
IEEE Micro's "Top Picks" special issue for papers "most relevant to industry and significant in contribution to the field of computer architecture" in 2007.
- [6] David I. August, Jonathan Chang, Sylvain Girbal, Daniel Gracia-Perez, Gilles Mouchard, David Penry, Olivier Temam, and Neil Vachharajani, "UNISIM: An Open Simulation Environment and Library for Complex Architecture Design and Collaborative Development," in *IEEE Computer Architecture Letters (CAL)*, September 2007.

- [7] George A. Reis, Jonathan Chang, and David I. August, “Automatic Instruction-Level Software-Only Recovery Methods,” in *IEEE Micro*, January 2007.
IEEE Micro’s “Top Picks” special issue for papers “most relevant to industry and significant in contribution to the field of computer architecture” in 2006.
- [8] Manish Vachharajani, Neil Vachharajani, David A. Penry, Jason A. Blome, Sharad Malik, and David I. August, “The Liberty Simulation Environment: A Deliberate Approach to High-Level System Modeling,” in *ACM Transactions on Computer Systems (TOCS)*, August 2006.
- [9] George A. Reis, Jonathan Chang, Neil Vachharajani, Ram Rangan, David I. August, and Shubhendu S. Mukherjee, “Software-Controlled Fault Tolerance,” in *ACM Transactions on Architecture and Code Optimization (TACO)*, December 2005.
- [10] Guilherme Ottoni, Ram Rangan, Adam Stoler, Matthew J. Bridges, and David I. August, “From Sequential Programs to Concurrent Threads,” in *IEEE Computer Architecture Letters (CAL)*, June 2005.
- [11] David I. August, Sharad Malik, Li-Shiuan Peh, Vijay Pai, Manish Vachharajani, and Paul Willmann, “Achieving Structural and Composible Modeling of Complex Systems,” in *The International Journal of Parallel Programming (IJPP)*, June 2005. Invited.
- [12] Spyridon Triantafyllis, Manish Vachharajani, and David I. August, “Compiler Optimization-Space Exploration,” in *The Journal of Instruction-level Parallelism (JILP)*, February 2005.
- [13] Manish Vachharajani, Neil Vachharajani, David A. Penry, Jason Blome, and David I. August, “The Liberty Simulation Environment, Version 1.0,” in *Performance Evaluation Review: Special Issue on Tools for Architecture Research (PER)*, March 2004. Invited.
- [14] Kevin Skadron, Margaret Martonosi, David I. August, Mark D. Hill, David J. Lilja, and Vijay S. Pai, “Challenges in Computer Architecture Evaluation,” in *IEEE Computer*, August 2003.
- [15] David I. August, Kurt Keutzer, Sharad Malik, and A. Richard Newton, “A Disciplined Approach to the Development of Platform Architectures,” in *Microelectronics Journal*, November 2002. Invited.
- [16] Wen-mei W. Hwu, David I. August, and John W. Sias, “Program Decision Logic Optimization using Predication and Control Speculation,” in *Proceedings of the IEEE*, November 2001.
- [17] David I. August, Wen-mei W. Hwu, and Scott A. Mahlke, “The Partial Reverse If-Conversion Framework for Balancing Control Flow and Predication,” in *International Journal of Parallel Programming (IJPP)*, October 1999. Invited.
Special issue composed of “outstanding papers” selected by the Program Committee of the 30th Annual ACM/IEEE International Symposium on Microarchitecture.
- [18] Wen-mei W. Hwu, Richard E. Hank, David M. Gallagher, Scott A. Mahlke, Daniel M. Lavery, Grant E. Haab, John C. Gyllenhaal, and David I. August, “Compiler Technology for Future Microprocessors,” in *Proceedings of the IEEE*, December 1995.

REFEREED CONFERENCE PUBLICATIONS

- [19] Jialu Huang, Arun Raman, Yun Zhang, Thomas B. Jablin, Tzu-Han Hung, and David I. August, “Decoupled Software Pipelining Creates Parallelization Opportunities,” to appear in *Proceedings of the 2010 International Symposium on Code Generation and Optimization (CGO)*, April 2010.
- [20] Arun Raman, Hanjun Kim, Thomas R. Mason, Thomas B. Jablin, and David I. August, “Speculative Parallelization Using Software Multi-threaded Transactions,” to appear in *Proceedings of the Fifteenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2010.
- [21] Easwaran Raman, Guilherme Ottoni, Arun Raman, Matthew Bridges, and David I. August, “Parallel-Stage Decoupled Software Pipelining,” in *Proceedings of the 2008 International Symposium on Code Generation and Optimization (CGO)*, April 2008.

- [22] Easwaran Raman, Neil Vachharajani, Ram Rangan, and David I. August, “Spice: Speculative Parallel Iteration Chunk Execution,” in *Proceedings of the 2008 International Symposium on Code Generation and Optimization (CGO)*, April 2008.
- [23] Guilherme Ottoni and David I. August, “Communication Optimizations for Global Multi-Threaded Instruction Scheduling,” in *Proceedings of the 13th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2008.
- [24] Guilherme Ottoni and David I. August, “Global Multi-Threaded Instruction Scheduling,” in *Proceedings of the 40th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2007.
- [25] Matthew J. Bridges, Neil Vachharajani, Yun Zhang, Thomas Jablin, and David I. August, “Revisiting the Sequential Programming Model for Multi-Core,” in *Proceedings of the 40th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2007.
Selected for IEEE Micro’s ”Top Picks” special issue for papers ”most relevant to industry and significant in contribution to the field of computer architecture” in 2007.
- [26] Neil Vachharajani, Ram Rangan, Easwaran Raman, Matthew J. Bridges, Guilherme Ottoni, and David I. August, “Speculative Decoupled Software Pipelining,” in *Proceedings of the 16th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2007.
- [27] Frances Perry, Lester Mackey, George A. Reis, Jay Ligatti, David I. August, and David Walker, “Fault-tolerant Typed Assembly Language,” in *Proceedings of the 2007 ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2007.
Winner Best Paper Award.
- [28] Bolei Guo, Neil Vachharajani, and David I. August, “Shape Analysis with Inductive Recursion Synthesis,” in *Proceedings of the ACM SIGPLAN 2007 Conference on Programming Language Design and Implementation (PLDI)*, June 2007.
- [29] Ram Rangan, Neil Vachharajani, Adam Stoler, Guilherme Ottoni, David I. August, and George Z. N. Cai, “Support for High-Frequency Streaming in CMPs,” in *Proceedings of the 39th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2006.
- [30] David Walker, Lester Mackey, Jay Ligatti, George A. Reis, and David I. August, “Static Typing for a Faulty Lambda Calculus,” in *Proceedings of the 11th ACM SIGPLAN International Conference on Functional Programming (ICFP)*, September 2006.
- [31] Jonathan Chang, George A. Reis, and David I. August, “Automatic Instruction-Level Software-Only Recovery Methods,” in *Proceedings of the International Conference on Dependable Systems and Networks (DSN)*, June 2006.
Winner of the William C. Carter Award.
Selected for IEEE Micro’s “Top Picks” special issue for papers “most relevant to industry and significant in contribution to the field of computer architecture” in 2006.
- [32] Matthew J. Bridges, Neil Vachharajani, Guilherme Ottoni, and David I. August, “Automatic Instruction Scheduler Retargeting by Reverse-Engineering,” in *Proceedings of the 2006 ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2006.
- [33] Spyridon Triantafyllis, Matthew J. Bridges, Easwaran Raman, Guilherme Ottoni, and David I. August, “A Framework for Unrestricted Whole-Program Optimization,” in *Proceedings of the 2006 ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2006.
- [34] Bolei Guo, Youfeng Wu, Cheng Wang, Matthew J. Bridges, Guilherme Ottoni, Neil Vachharajani, Jonathan Chang, and David I. August, “Selective Runtime Memory Disambiguation in a Dynamic Binary Translator,” in *Proceedings of the 15th International Conference on Compiler Construction (CC)*, March 2006.
- [35] David A. Penry, Daniel Fay, David Hodgdon, Ryan Wells, Graham Schelle, David I. August, and Daniel A. Connors, “Exploiting Parallelism and Structure to Accelerate the Simulation of Chip Multi-processors,” in *Proceedings of the Twelfth International Symposium on High-Performance Computer Architecture (HPCA)*, February 2006.

- [36] Guilherme Ottoni, Ram Rangan, Adam Stoler, and David I. August, “Automatic Thread Extraction with Decoupled Software Pipelining,” in *Proceedings of the 38th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, November 2005.
One of five papers nominated for the Best Paper Award by the Program Committee.
- [37] Guilherme Ottoni, Ram Rangan, Adam Stoler, and David I. August, “A New Approach to Thread Extraction for General-Purpose Programs,” in *Proceedings of the 2nd Watson Conference on Interaction between Architecture, Circuits, and Compilers (PAC2)*, September 2005.
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