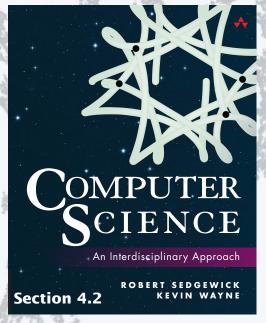


COMPUTER SCIENCE SEDGEWICK/WAYNE

PART II: ALGORITHMS, THEORY, AND MACHINES



http://introcs.cs.princeton.edu

Questions for discussion Part II



Search in an array

Suppose that an array of strings contains

a[0] black raspberry

a[1] chocolate

a[2] cookie dough

a[3] coffee

a[4] mint

a[5] strawberry

a[6] vanilla

- Q. How many compares for a successful search for mint using:
 - binary search?
 - sequential search?
- Q. How many compares for an unsuccessful search for pistachio using:
 - binary search?
 - sequential search?

Sorting performance

Q. The following tables are performance results for algorithms that sort 10-character strings. Label each as *insertion sort* or *mergesort*.

N	T _N	T _N /T _{N/2}
20,000	1	_
40,000	4	_
80,000	35	
160,000	225	

N	T _N	$T_N/T_{N/2}$
1 million	1	_
2 million	2	_
4 million	5	
8 million	10	

Sorting and searching performance

Q. To the right of each option, fill in the circle corresponding to the one-word characterization that best describes the order of growth of the *worst-case* running time.

	logarithmic	linear	linearithmic	quadratic
mergesort	\bigcirc	\bigcirc	\bigcirc	\bigcirc
merge		\bigcirc		\bigcirc
binary search	\bigcirc	\bigcirc	\bigcirc	
insertion sort	\bigcirc	\bigcirc	\bigcirc	\bigcirc
sequential search		\bigcirc		\bigcirc
bubble sort	\bigcirc		\bigcirc	

Lecture 12: Stacks and Queues

Pushdown stack

- Q. In the following, interpret
 - a letter to mean *push*
 - a minus sign to mean pop
 - 1. Starting with an empty stack, give the contents of the stack after

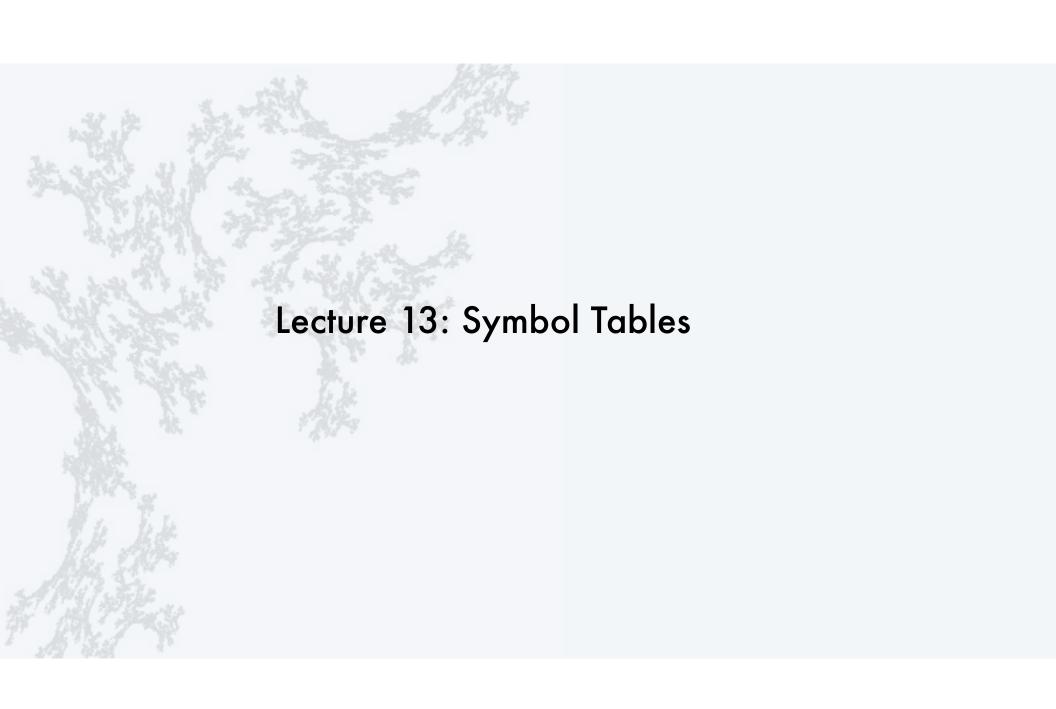
$$a - b c - d e - f g h - - i$$

2. Suppose that the standard array representation was used for the stack. Give the contents of the *array* after

$$a - b c - d e - f g h - - i$$

Prefix/infix

Q. Give an *infix* expression corresponding to each of the following *prefix* expressions.



Sorting and searching performance

Q. To the right of each option, fill in the circle corresponding to the one-word characterization that best describes the order of growth of the *worst-case* running time.

	logarithmic	linear	linearithmic	quadratic
mergesort	\bigcirc	\bigcirc	\bigcirc	\bigcirc
merge		\bigcirc	\bigcirc	
binary search	\bigcirc	\bigcirc	\bigcirc	\bigcirc
BST search	O 10%	O 23%	O 22%	O 38%
insertion sort		\bigcirc	\bigcirc	
sequential search	\bigcirc	\bigcirc	\bigcirc	\bigcirc
bubble sort	\bigcirc			

Searching scalability

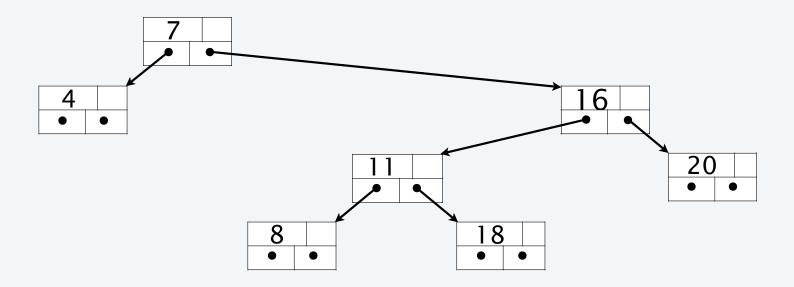
Q. An algorithm is *scalable* if it can accommodate an unpredictable mix of operations for a large amount of data, even as the amount of data grows.

Which of the following data structures admits scalable symbol-table algorithms?

	scalable?
array	
linked list	\bigcirc
BST	\bigcirc

Legal BST

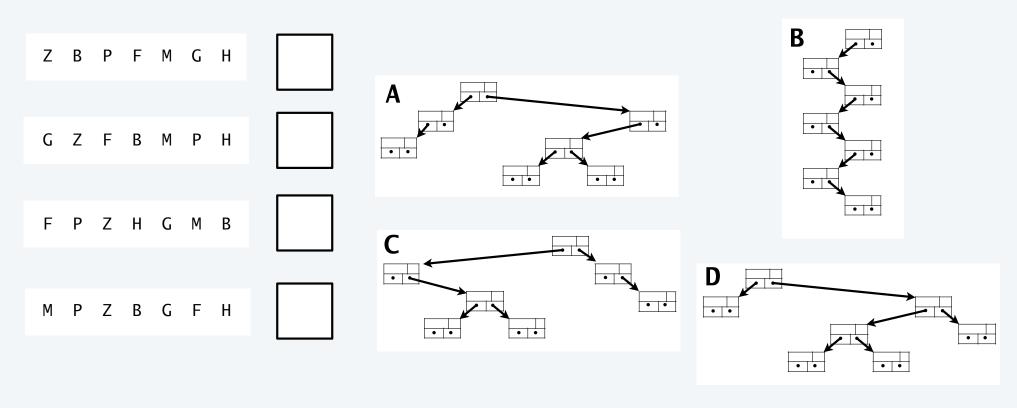
Q. Is this a BST?



A. No.

BST construction

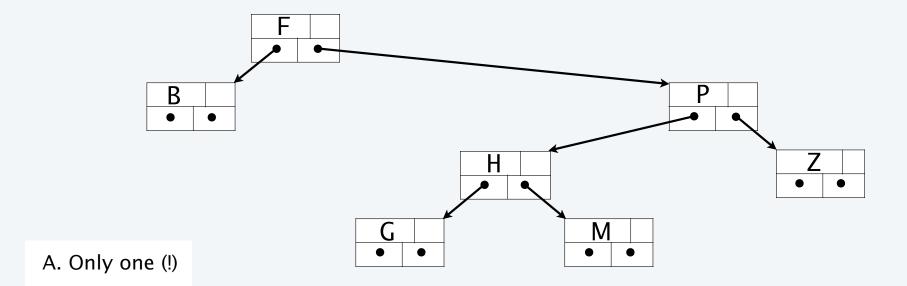
Q. Match the key sequences with the BST produced by inserting them in order into an initially empty tree.



Tree labeling

Q. How many ways to assign N keys to a give N-node tree?

 $\mathsf{B} \quad \mathsf{F} \quad \mathsf{G} \quad \mathsf{H} \quad \mathsf{M} \quad \mathsf{P} \quad \mathsf{Z}$



Tree height

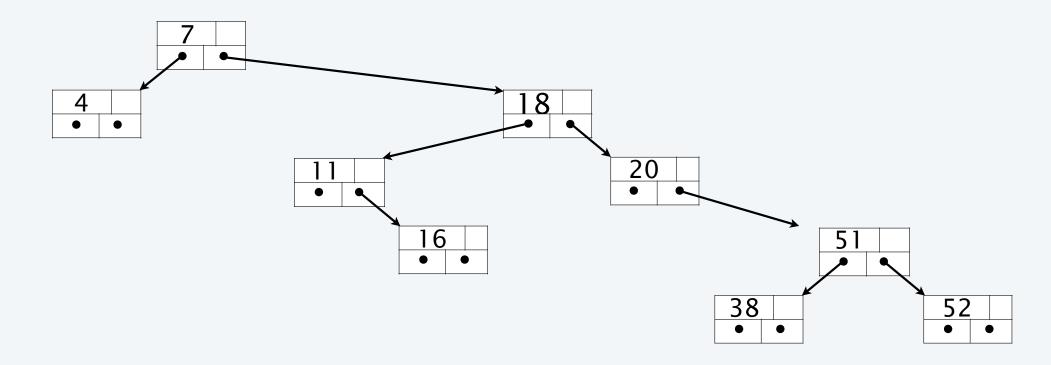
Q. Give the *height* of the BST produced by inserting keys in the order given into an initially empty BST.

Tree sequences

Q. Which of the following could *not* have been the sequence of keys examined to search for 70 in a BST?

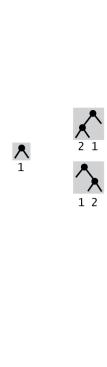
Order statistics

Q. Identify the smallest, largest, and median.



Tree enumeration

Q. How many different trees of 3 nodes? 4?



Lecture 14: Intro to Theory of Computing

REs

Q. How do know what language is described by an RE?

Ex. Fall 2014 Question 5.

Let L = { ab, aaab, aaaab, aabaaab, aabaaab }.

Write 1, 2, 3, or 4 to indicate whether the RE

- 1. Matches no strings in L.
- 2. Matches *only some strings in L* and some other strings.
- 3. Matches all strings in L and some other strings.
- 4. Matches all strings in L and no other strings.

(aa*b)*	3	
a*b*	2	
(a b)*ab	3	
a*baba*b*		
(ab) (a(a aba)(a aa)b)	4	
a*baaa*b*	2	

Q. Match the REs with the DFAs.

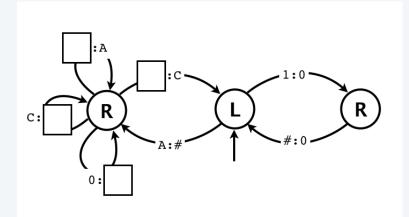
a*|(a*ba*ba*ba*)* B (ab)* В C (a*b)+ D ba*

Lecture 15: Turing Machines

Tracing TMs

Q. How do we trace a Turing Machine?

Ex. Fall 2014 Question 5.



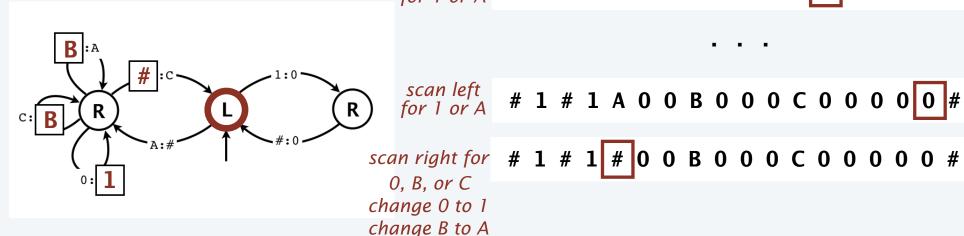
This TM uses the symbols A, B, and C to delineate the two most recently computed Fibonacci numbers. Here is the tape before computing Fibonacci number 5, with the tape head positioned at the C:

1 # 1 A 1 1 B 1 1 1 C # # # # #

Fill in exactly one symbol in each of the 4 empty boxes to complete the design of this TM. You may assume that the initial contents of the tape and the position of the tape head are as given above and that the machine starts in the middle state.

Q. How do we trace a TM?

Ex. Fall 2014 Question 5.



change C to B

scan left # 1 # 1 A 1 1 B 1 1 1 C # # # # # for 1 or A scan right for # # 1 # 1 A 1 1 B 1 1 0 C # # # # # scan left for 1 or A # 1 # 1 A 1 1 B 1 1 0 C 0 # # # # #

scan right for # 1 # 1 # 0 0 B 0 0 0 C 0 0 0 0 #

scan left # 1 # 1 # 1 1 A 1 1 1 B 1 1 1 1 1 C # for 1 or A

Computability

Spring 2015 Q5

	Turing Machine	TOY with sufficient memory	DFA	None of these
Can perform any possible computation (if the Church-Turing thesis holds).	✓	✓	X	X
Cannot express some Java programs	X	X	1	X
Cannot be simulated in Java	X	X	X	✓
Always halts on all finite inputs	X	X	√	X
Can always correctly check whether an arbitrary Java program goes into a loop.	X	X	X	1

Computability

Spring 2011 Q8

A	known to be true	There exists a mathematical function that can be computed in Java, but <i>cannot</i> be computed on a Turing machine.	В
В	known to be false	There exists a mathematical function that can be computed in polynomial time on a quantum computer, but cannot be	D
C	if true would falsify the Church-Turing thesis	computed in polynomial time on a Turing machine. Assume that quantum computers can be built.	
D	if true would falsify the extended Church- Turing thesis	There exists a mathematical function that can be computed in polynomial time in Java, but <i>cannot</i> be computed in polynomial time on a Turing machine.	В
E	if true would prove the Church-Turing thesis		
		There exists a Turing machine that can simulate the behavior of any other Turing machine.	A

Lecture 16: Intractability

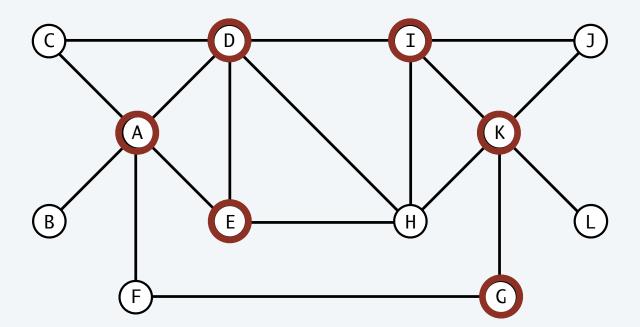
Polynomial vs. Exponential

Circle the largest value, for $N = 10$	N 100	1000 <i>N</i> ³	2 ^N
Circle the largest value, for $N = 100$	N 100	1000 <i>N</i> ³	2 <i>N</i>
Circle the largest value, for $N = 1000$	N 100	1000 <i>N</i> ³	2 <i>N</i>

Vertex cover

Exercise 5.5.6

Find a minimum-cardinality vertex cover for this graph.



NP-hard vs. NP-complete

- Q. If someone finds a polynomial-time algorithm for FACTOR, would that prove that P = NP?
- A. No. (No reduction from an-NP-complete problem is known.)
- Q. If someone finds a polynomial-time algorithm for MIN VERTEX COVER, would that prove that P = NP?
- A. Yes. Such a solution would give a solution to VERTEX COVER, which is NP-complete.
- Q. If someone proves that P=NP, would that give a polynomial-time algorithm for FACTOR?
- A. No. It would prove that one exists, not necessarily exhibit one.
- Q. If someone proves that P=NP, would that give a polynomial-time algorithm for MIN VERTEX COVER?
- A. No. (It is "NP-hard" but not known to be in NP.)

NP-completeness

Exercise 5.5.25

Which of the following can we infer from the fact that TSP is NP-complete, if we assume that $P \neq NP$?

- a. No algorithm exists that solves arbitrary instances of TSP.
- b. No algorithm exists that *efficiently* solves arbitrary instances of TSP.
- c. There exists an algorithm that efficiently solves arbitrary instances of TSP, but no one has been able to find it.
- d. TSP is not in P.
- e. All algorithms that are guaranteed to solve TSP run in polynomial time for some family of inputs.
- f. All algorithms that are guaranteed to solve TSP run in exponential time for all families of inputs.

- exponential algorithm would do
- / that's the point
- χ it would prove P = NP
- same as b.
- X nonsense distractor
- **X** could be between poly and exp

NP-completeness

Exercise 5.5.29

f. If A is in P, then B is in P.

g. If B is in P, then A is in P.

polynomial-time reduces to B. Which of the following can we infer?

a. If B is NP-complete then so is A.

b. If A is NP-complete then so is B.

c. If B is NP-complete and A is in NP then A is NP-complete.

d. If A is NP-complete and B is in NP then B is NP-complete.

e. A and B cannot both be NP-complete.

why not?

Let A and B be two *decision* problems. Suppose we know that A

wrong way

an implication that matters

P vs. NP

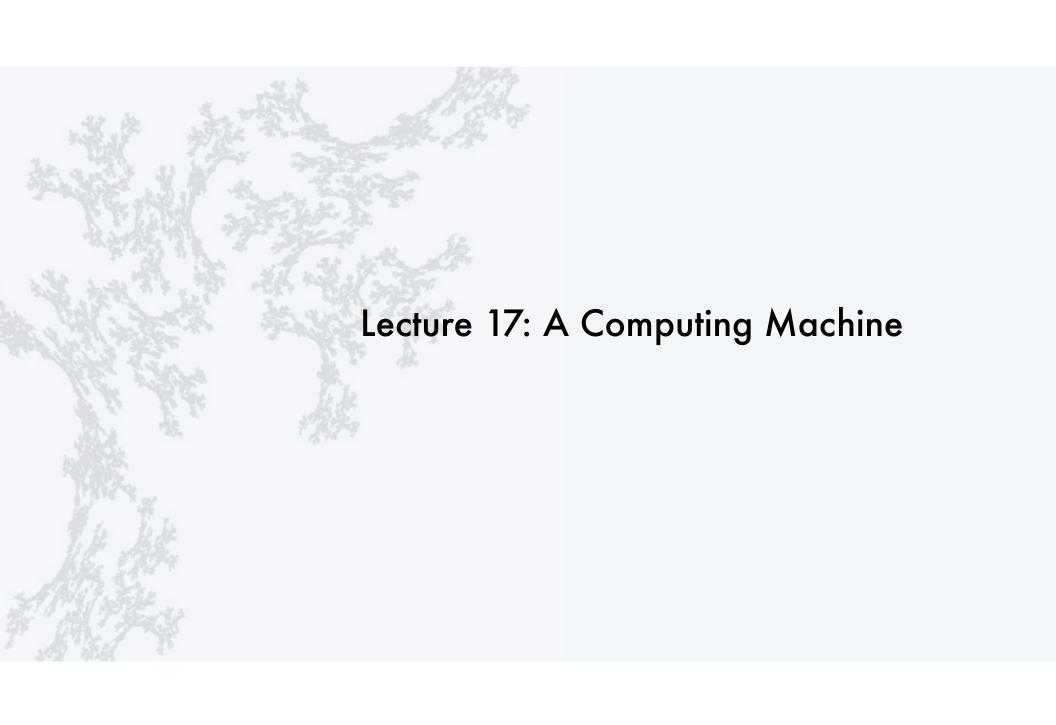
Q. Assume that P = NP. Check all correct options.

	halting problem	TSP	SAT	FACTOR	ILP
is computable		\bigcirc			\bigcirc
is intractable		\bigcirc			\bigcirc
is in P		\checkmark			\bigcirc
is in NP		\bigcirc			\bigcirc
is in NPC	\bigcirc	\bigcirc			\bigcirc

P vs. NP

Q. Assume that $P \neq NP$. Check all correct options.

	halting problem	TSP	SAT	FACTOR	ILP
is computable			\bigcirc		\bigcirc
is intractable			\bigcirc		\bigcirc
known to be in P					\bigcirc
known to be in NP		\checkmark			\bigcirc
known to be NPC	\bigcirc		\bigcirc		







Binary operations

Q. Why is ~ 0 equal to -1 and not 1? (Fall 2014 Q1B)

```
A (wrong).

~ is "not"

0 is "false"

"not false" is "true"

"true" is 1
```

Representing numbers

Q. Fill in the blanks in this table.

unsigned base 10	16-bit binary	4-digit hex
100	000000001100100	0064
4096+256+16+1 = 4369	000100010001	1111
12	00000000001100	000C

Representing information

Q. Fill in the blanks in this table.

hex	TOY instruction	TOY integer
0064	halt	100
1A00	R[A] = R[0] + R[0]	6,656
FFF0	R[F] = PC + 1; PC = F0	-16
2111	R[1] = R[1] - R[1]	8,465
DEEF	if (R[E] > 0) PC = EF	-8,465

opcode	operation	format	pseudo-code
0	halt	_	halt
1	add	RR	R[d] = R[s] + R[t]
2	subtract	RR	R[d] = R[s] - R[t]
3	bitwise and	RR	R[d] = R[s] & R[t]
4	bitwise xor	RR	$R[d] = R[s] \land R[t]$
5	shift left	RR	$R[d] = R[s] \ll R[t]$
6	shift right	RR	$R[d] = R[s] \gg R[t]$
7	load addr	Α	R[d] = addr
8	load	Α	R[d] = M[addr]
9	store	Α	M[addr] = R[d]
Α	load indirect	RR	R[d] = M[R[t]]
В	store indirect	RR	M[R[t]] = R[d]
C	branch zero	Α	if $(R[d] == 0)$ PC = addr
D	branch positive	Α	if $(R[d] > 0)$ PC = addr
E	jump register	RR	PC = R[d]
F	jump and link	Α	R[d] = PC + 1; PC = addr

TOY blocking and tackling I

Q. Give seven instructions (all having different opcodes) to put 0000 in R[A].

1A00 R[A] = R[0] + R[0]

2Axx R[A] = R[x] - R[x]

3A0x R[A] = R[0] & R[x]

4Axx R[A] = R[x]
$$\wedge$$
 R[x]

5A0x R[A] = R[0] $<<$ R[0]

6A0x R[A] = R[0] $>>$ R[x]

7A00 R[A] = 0000

opcode	operation	format	pseudo-code
0	halt	_	halt
1	add	RR	R[d] = R[s] + R[t]
2	subtract	RR	R[d] = R[s] - R[t]
3	bitwise and	RR	R[d] = R[s] & R[t]
4	bitwise xor	RR	$R[d] = R[s] \land R[t]$
5	shift left	RR	$R[d] = R[s] \ll R[t]$
6	shift right	RR	$R[d] = R[s] \gg R[t]$
7	load addr	Α	R[d] = addr
8	load	Α	R[d] = M[addr]
9	store	Α	M[addr] = R[d]
Α	load indirect	RR	R[d] = M[R[t]]
В	store indirect	RR	M[R[t]] = R[d]
C	branch zero	Α	if $(R[d] == 0)$ PC = addr
D	branch positive	Α	if $(R[d] > 0)$ PC = addr
E	jump register	RR	PC = R[d]
F	jump and link	Α	R[d] = PC + 1; PC = addr

TOY blocking and tackling II

Q. Which of the following put FFFF in R[A]?

7AFF	X	R[A] = 00FF
7B01 2A0B	√	R[B] = 0001 R[A] = R[0] - R[B]
7A01 2A0A	1	R[A] = 0001 R[A] = R[0] - R[A]
7AFF 7B08	√	R[A] = 00FF R[B] = 0008
5AA8 6AA8		R[A] = R[A] << R[B] R[A] = R[A] >> R[B]

opcode	operation	format	pseudo-code
0	halt	_	halt
1	add	RR	R[d] = R[s] + R[t]
2	subtract	RR	R[d] = R[s] - R[t]
3	bitwise and	RR	R[d] = R[s] & R[t]
4	bitwise xor	RR	$R[d] = R[s] \land R[t]$
5	shift left	RR	$R[d] = R[s] \ll R[t]$
6	shift right	RR	$R[d] = R[s] \gg R[t]$
7	load addr	Α	R[d] = addr
8	load	Α	R[d] = M[addr]
9	store	Α	M[addr] = R[d]
Α	load indirect	RR	R[d] = M[R[t]]
В	store indirect	RR	M[R[t]] = R[d]
C	branch zero	Α	if $(R[d] == 0)$ PC = addr
D	branch positive	Α	if $(R[d] > 0)$ PC = addr
E	jump register	RR	PC = R[d]
F	jump and link	Α	R[d] = PC + 1; PC = addr

TOY code I

Q. What does this TOY program do?

10: 82FF R[2] = stdin

11: 7B01 R[B] = 0001

12: 2A0B R[A] = FFFF

13: 432A $R[3] = R[2] \land R[A]$

14: 133B R[3] = R[3] + 1

15: 93FF stdout = R[3]

16: 0000 halt

opcode	operation	format	pseudo-code
0	halt	_	halt
1	add	RR	R[d] = R[s] + R[t]
2	subtract	RR	R[d] = R[s] - R[t]
3	bitwise and	RR	R[d] = R[s] & R[t]
4	bitwise xor	RR	$R[d] = R[s] \land R[t]$
5	shift left	RR	$R[d] = R[s] \ll R[t]$
6	shift right	RR	$R[d] = R[s] \gg R[t]$
7	load addr	Α	R[d] = addr
8	load	Α	R[d] = M[addr]
9	store	Α	M[addr] = R[d]
Α	load indirect	RR	R[d] = M[R[t]]
В	store indirect	RR	M[R[t]] = R[d]
C	branch zero	Α	if $(R[d] == 0)$ PC = addr
D	branch positive	Α	if $(R[d] > 0)$ PC = addr
E	jump register	RR	PC = R[d]
F	jump and link	Α	R[d] = PC + 1; PC = addr

TOY code II

Q. What does this TOY program do?

```
10: 8210 R[2] = 8210
```

11: 7D01
$$R[D] = 0001$$

12:
$$2AOD$$
 $R[A] = FFFF$

13: 432A
$$R[3] = 7DEF$$

14: 9315
$$M[15] = R[3]$$

17: 0000 halt

opcode	operation	format	pseudo-code
0	halt	_	halt
1	add	RR	R[d] = R[s] + R[t]
2	subtract	RR	R[d] = R[s] - R[t]
3	bitwise and	RR	R[d] = R[s] & R[t]
4	bitwise xor	RR	$R[d] = R[s] \land R[t]$
5	shift left	RR	$R[d] = R[s] \ll R[t]$
6	shift right	RR	$R[d] = R[s] \gg R[t]$
7	load addr	Α	R[d] = addr
8	load	Α	R[d] = M[addr]
9	store	Α	M[addr] = R[d]
Α	load indirect	RR	R[d] = M[R[t]]
В	store indirect	RR	M[R[t]] = R[d]
C	branch zero	Α	if $(R[d] == 0)$ PC = addr
D	branch positive	Α	if $(R[d] > 0)$ PC = addr
E	jump register	RR	PC = R[d]
F	jump and link	Α	R[d] = PC + 1; PC = addr



TOY blocking and tackling III

Q. (F11) Suppose that R[2] contains a small integer x. Match each instruction with a description of the value of R[2] after it is executed.

1000	G
4222	A
1222	В
5222	Ε
E022	G
7022	G
1202	G

Α		0
A	•	U

$$\mathbf{C}$$
. \mathbf{x}^2

F.
$$x - 2$$

H. No match

opcode	operation	format	pseudo-code
0	halt	_	halt
1	add	RR	R[d] = R[s] + R[t]
2	subtract	RR	R[d] = R[s] - R[t]
3	bitwise and	RR	R[d] = R[s] & R[t]
4	bitwise xor	RR	$R[d] = R[s] \land R[t]$
5	shift left	RR	$R[d] = R[s] \ll R[t]$
6	shift right	RR	$R[d] = R[s] \gg R[t]$
7	load addr	Α	R[d] = addr
8	load	Α	R[d] = M[addr]
9	store	Α	M[addr] = R[d]
Α	load indirect	RR	R[d] = M[R[t]]
В	store indirect	RR	M[R[t]] = R[d]
C	branch zero	Α	if $(R[d] == 0)$ PC = addr
D	branch positive	Α	if $(R[d] > 0)$ PC = addr
E	jump register	RR	PC = R[d]
F	jump and link	Α	R[d] = PC + 1; PC = addr

TOY code with a loop I

Q. [S11] Consider this TOY program.

20: 2AAB R[A] = R[A] - R[B]

21: DA20 if (R[A] > 0) PC = 20

22: CA24 if (R[A] == 0) PC = 24

23: 1AAB R[A] = R[A] + R[B]

24: 0000 halt

A. Give the result when R[A] is 001A and R[B] is 0008.

R[A]: **0002** R[B]: **0008**

B. Give the result when R[A] is 5EAB and R[B] is 0010.

R[A]: **000B** R[B]: **0010**

C. Give equivalent Java code.	a = a % b
	00 70 20

opcode	operation	format	pseudo-code
0	halt	_	halt
1	add	RR	R[d] = R[s] + R[t]
2	subtract	RR	R[d] = R[s] - R[t]
3	bitwise and	RR	R[d] = R[s] & R[t]
4	bitwise xor	RR	$R[d] = R[s] \land R[t]$
5	shift left	RR	$R[d] = R[s] \ll R[t]$
6	shift right	RR	$R[d] = R[s] \gg R[t]$
7	load addr	Α	R[d] = addr
8	load	Α	R[d] = M[addr]
9	store	Α	M[addr] = R[d]
Α	load indirect	RR	R[d] = M[R[t]]
В	store indirect	RR	M[R[t]] = R[d]
C	branch zero	Α	if $(R[d] == 0)$ PC = addr
D	branch positive	Α	if $(R[d] > 0)$ PC = addr
E	jump register	RR	PC = R[d]
F	jump and link	Α	R[d] = PC + 1; PC = addr

TOY code with a loop II

Q. [S2012] What does this TOY program punch?

```
OF: 000N
10: 840F   R[4] = M[0F]
11: 4555   R[5] = 0000
12: 7601   R[6] = 0001
13: 1554   R[5] = R[5] + R[4]
14: 2446   R[4] = R[4] - 1
15: D413   if (R[4] > 0) PC = 13
16: 95FF   stdout = R[5]
17: 0000   halt
```

A. $N + (N -$	(-1) + (N-2)	$+ \ldots + 1 = N(N + 1)/2$
---------------	--------------	-----------------------------

Q. Largest value in 0F with no overflow?

A. 0100

opcode	operation	format	pseudo-code
0	halt	_	halt
1	add	RR	R[d] = R[s] + R[t]
2	subtract	RR	R[d] = R[s] - R[t]
3	bitwise and	RR	R[d] = R[s] & R[t]
4	bitwise xor	RR	$R[d] = R[s] \land R[t]$
5	shift left	RR	$R[d] = R[s] \ll R[t]$
6	shift right	RR	$R[d] = R[s] \gg R[t]$
7	load addr	Α	R[d] = addr
8	load	Α	R[d] = M[addr]
9	store	Α	M[addr] = R[d]
Α	load indirect	RR	R[d] = M[R[t]]
В	store indirect	RR	M[R[t]] = R[d]
C	branch zero	Α	if $(R[d] == 0)$ PC = addr
D	branch positive	Α	if $(R[d] > 0)$ PC = addr
E	jump register	RR	PC = R[d]
F	jump and link	Α	R[d] = PC + 1; PC = addr

TOY code with a loop III

Q. [Ex. 6.3.21] What does this TOY program punch?

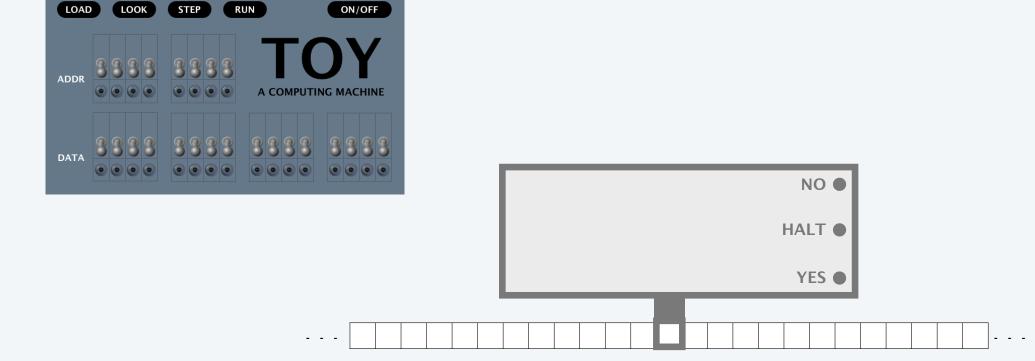
10: 7101	R[1] = 0001	DO:	0001
11: 72D0	R[2] = 00D0	D1:	00D6
12: 1421	R[4] = R[2] + R[1]	D2:	0005
13: A302	R[3] = M[R[2]]	D3:	00D8
14: 93FF	stdout = R[3]	D4:	0004
15: A204	R[2] = M[R[4]]	D5:	00D2
16: D212	if $(R[2] > 0) PC = 12$	D6:	0002
17: 0000	halt	D7:	00DA
		D8:	0006
		D9:	0000
A. 0001 0002	0003 0004 0005 0006	DA:	0003

DB: 00D4

opcode	operation	format	pseudo-code
0	halt	_	halt
1	add	RR	R[d] = R[s] + R[t]
2	subtract	RR	R[d] = R[s] - R[t]
3	bitwise and	RR	R[d] = R[s] & R[t]
4	bitwise xor	RR	$R[d] = R[s] \land R[t]$
5	shift left	RR	$R[d] = R[s] \ll R[t]$
6	shift right	RR	$R[d] = R[s] \gg R[t]$
7	load addr	Α	R[d] = addr
8	load	Α	R[d] = M[addr]
9	store	Α	M[addr] = R[d]
Α	load indirect	RR	R[d] = M[R[t]]
В	store indirect	RR	M[R[t]] = R[d]
C	branch zero	Α	if $(R[d] == 0)$ PC = addr
D	branch positive	Α	if $(R[d] > 0)$ PC = addr
E	jump register	RR	PC = R[d]
F	jump and link	Α	R[d] = PC + 1; PC = addr

Key idea I

Q. Can a TOY do anything that a UTM can (and vice-versa)?



Key idea II

Q. Can a TOY do anything that your computer can (and vice-versa)?





Lecture 19: Combinational Circuits

Boolean logic I

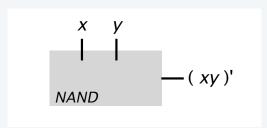
Q. [Ex. 7.1.3] Give a truth-table proof showing that x + yz = (x + y)(x + z).

A.

X	У	Z	yz	x + yz	x + y	X + Z	(x + y) (x + z)
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0
0	1	0	0	0	1	0	0
0	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1
1	0	1	0	1	1	1	1
1	1	0	0	1	1	1	1
1	1	1	1	1	1	1	1

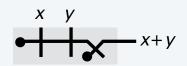
NAND gate

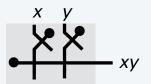
Q. Give a circuit that implements the NAND function.



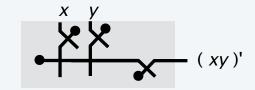
X	У	NAND
0	0	1
0	1	1
1	0	1
1	1	0

Hints.



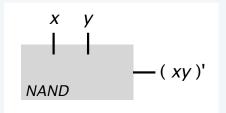


A.

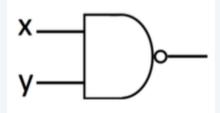


Notation

Q. Why this?



and not this?



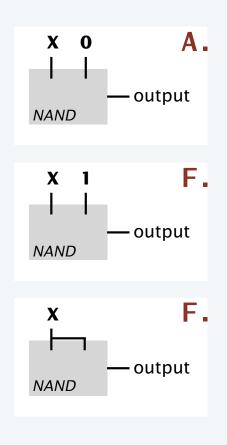
A.

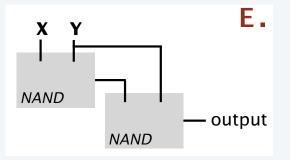


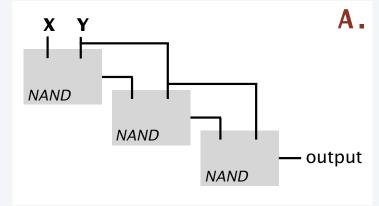
A. Eliminates a layer of abstraction (stay tuned).

Simple circuits I

Q. [Spring 2014] Label each circuit with the letter corresponding to its output.



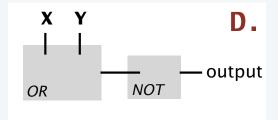


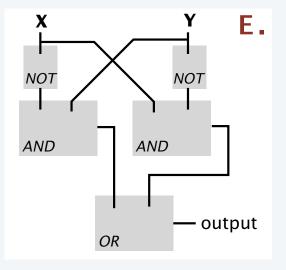


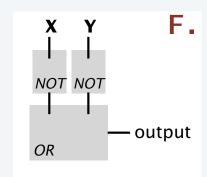
- **A.** 1
- **B.** 0
- **C.** xy
- **D.** x'y'
- **E.** xy + y'
- **F.** x'

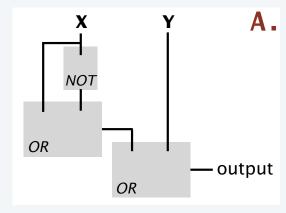
Simple circuits II

Q. [Spring 2013] Label each circuit with the letter corresponding to its output.









- A. always 1
- **B.** always 0
- **C.** 1 iff X and Y are equal
- **D.** 1 iff X and Y are both 0
- E. 1 iff X and Y are not equal
- **F.** 0 iff X and Y are both 1

Boolean logic II

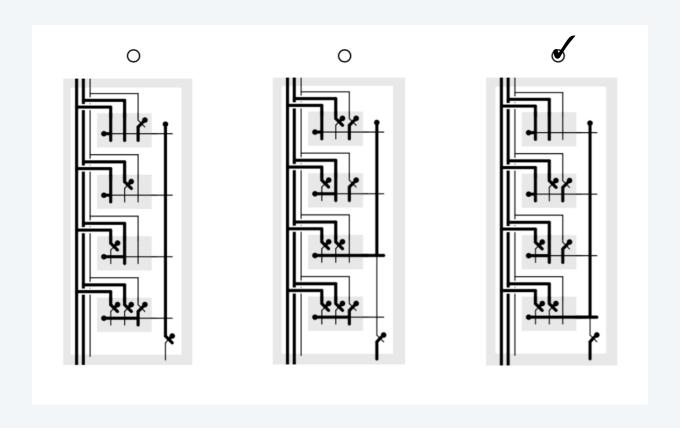
Q. [F 2014] Give a truth table for EVEN PARITY (number of 1s in inputs is even).

A.

X	У	Z	EVEN PARITY
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Combinational circuit

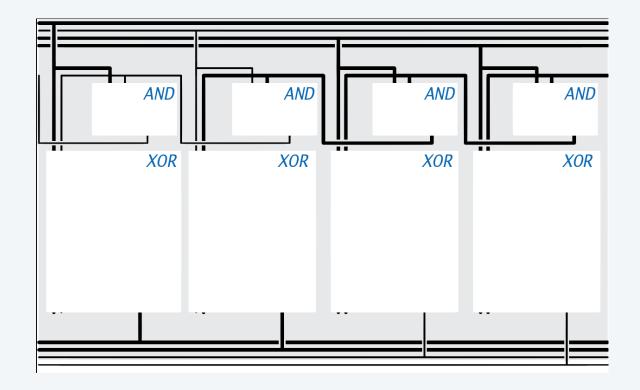
Q. [F 2014] Which circuit is computing EVEN PARITY for 1 1 0?



Incrementer

Q. [7.3.18] Draw a circuit that *increments* a 4-bit number.

Xi $C_i \quad C_{i+1}$ carry bit X_i C_i Z_i sum bit



Incrementer

Q. [7.3.18] Draw a circuit that *increments* a 4-bit number.

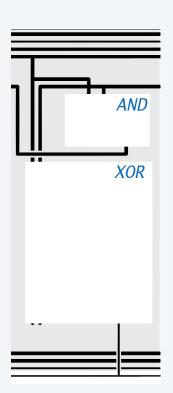
A.

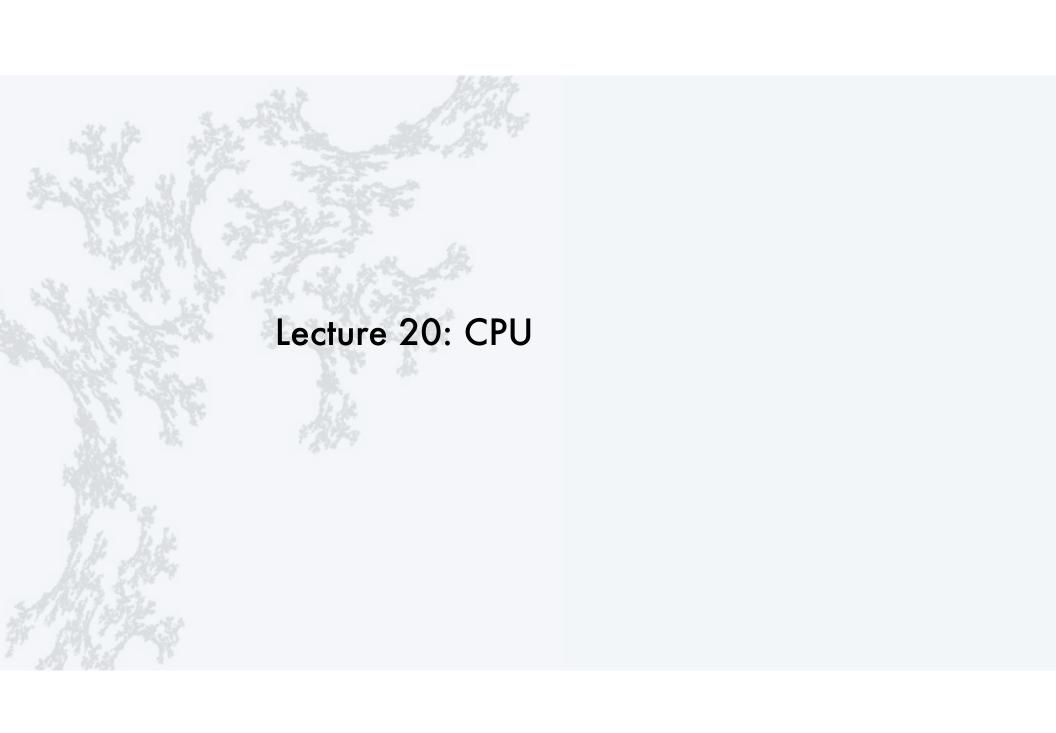
C 4	C 3	C 2	<i>C</i> ₁	1
	X 3	X 2	X 1	X 0
	Z 3	Z 2	Z 1	Z 0

carry bit

sum bit

Xi	Ci	C i+1
0	0	0
0	1	0
1	0	0
1	1	1
Xi	Ci	Zi
<i>X_i</i> 0	<i>C_i</i> 0	<i>Z</i> _i
		Ī
0	0	0





Number representation

Q. (Spring 2013 Q1) Why can 3/2 be represented as an exact double in Java but 1/10 cannot?

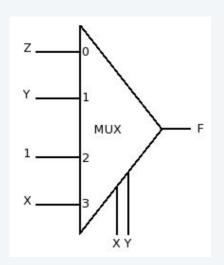
A. No questions on floating point representation in this exam.

A. 3/2 = 1 + 1/2, but no way to represent 1/10 as sum of decreasing powers of 1/2.

Circuit components

- Q. (Spring 2012 Q5) How to write the truth table?
- A. Try all possibilities.

A *multiplexer* switches the addressed input value to the output (p. 942)



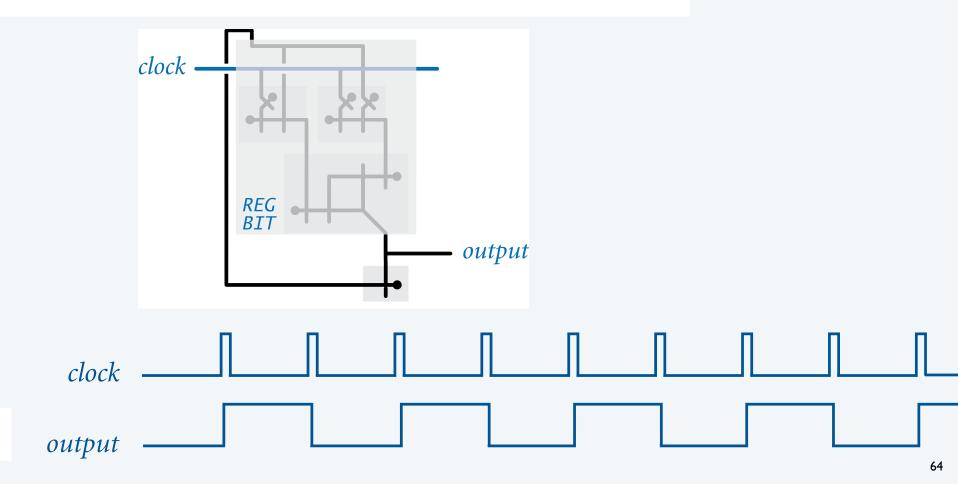
У	Z	f
0	0	0
0	1	1
1	0	1
1	1	1
0	0	1
0	1	1
1	0	1
1	1	1
	0 0 1 1 0 0	0 0 0 1 1 0 0 0 0 1 1 0

- Q. Do we need to memorize what the complex circuits are composed of?
- A. No, you need to know what they do.

Sequential circuit I

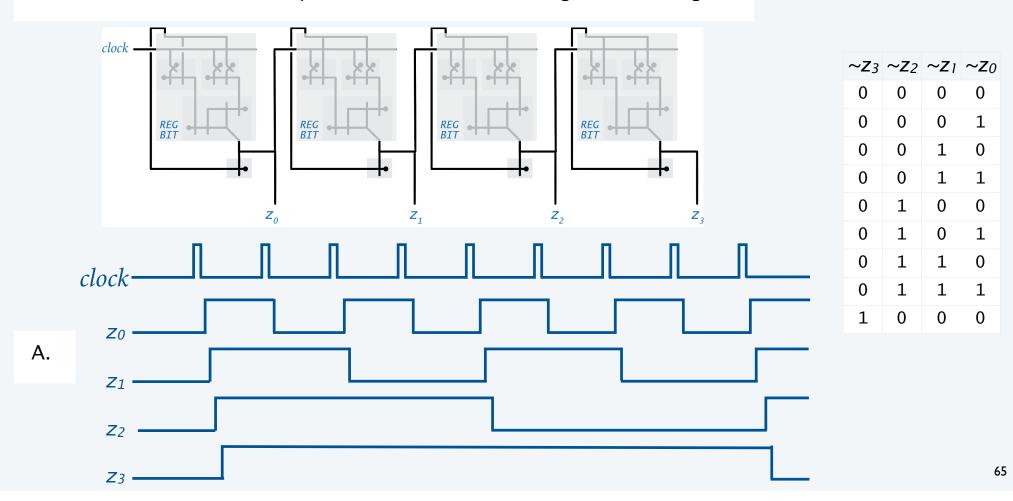
A.

Q. (Ex. 7.4.3) Draw the response of this circuit to the given clock signal.



Sequential circuit II

Q. (Ex. 7.4.16) Draw the response of this circuit to the given clock signal.



Matching I

Q. (Fall 2014 Q10) Identify each of the CPU components as combinational or sequential.

	combinational	sequential
ADDR MUX	\checkmark	\bigcirc
ALU	\checkmark	
CLOCK	\bigcirc	
CONTROL	\checkmark	\bigcirc
IR	\bigcirc	
MEMORY	\bigcirc	
PC	\bigcirc	
R	\bigcirc	
R MUX	\bigcirc	\bigcirc

Matching II

Q. (Fall 2014 Q10, modified) Match each CPU component to a description.

ADDR MUX B.

ALU .

CLOCK H.

CONTROL D.

IR G

MEMORY F.

PC A.

R C.

R MUX

A. holds address of current instruction

B. inputs from IR and PC

C. contents ultimately come from one of three sources

D. decodes instructions

E. selects register inputs

F. big sequential circuit

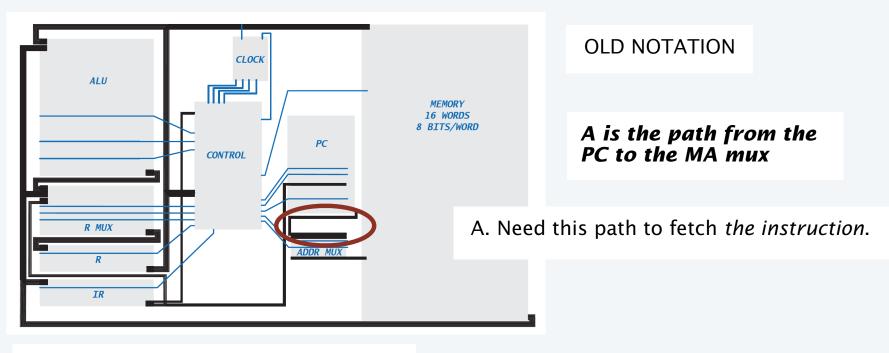
G. holds current instruction

H. sequential circuit that produces periodic pulses

I. computes boolean function values

Data paths I

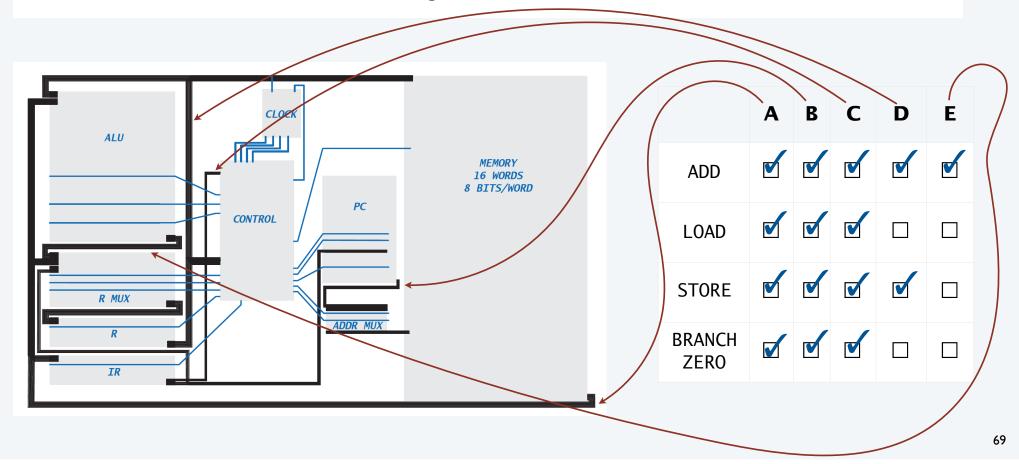
Q. (Spring 2015 Q7) Why is A checked as a needed data path for every instruction?



- Q. How do we study from Lecture 20?
- A. Read Chapter 7.

Data paths

Q. (Spring 2015 Q7) Check all the boxes that correspond to the datapaths needed to fetch and execute the following TOY-8 instructions.



TOY-8 CPU

