Memory; Sequential & Clocked Circuits; Finite State Machines

COS 116: 3/27/2007

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Combinational circuit: addition

	25	11001
+	29	11101
	54	110110

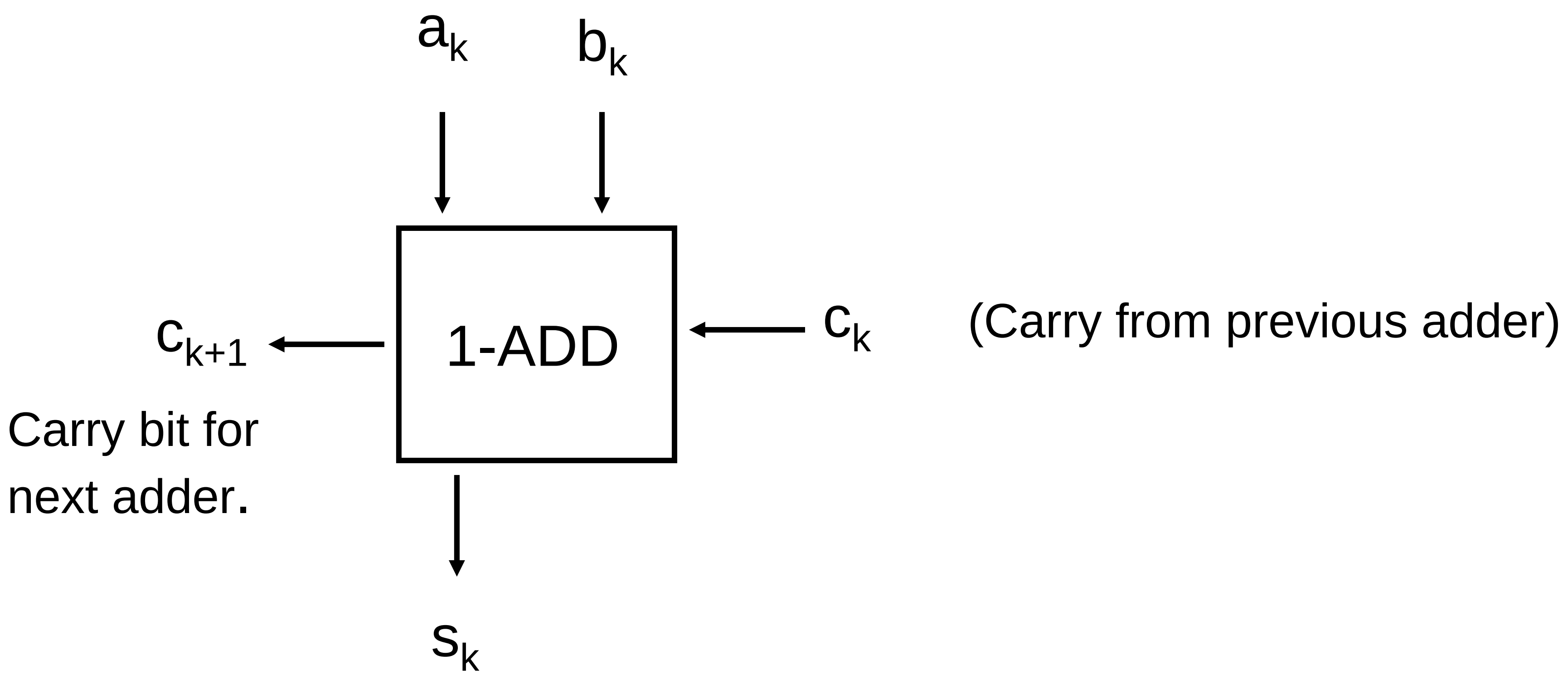
- Want to any two *N*-bit integers

Modular design

$$
\begin{array}{cccccccl}
 & & c_{N-1} & c_{N-2} & \dots & c_1 & c_0 & \text{Carry bits} \\
 & & a_{N-1} & a_{N-2} & \dots & a_1 & a_0 & \\
+ & & b_{N-1} & b_{N-2} & \dots & b_1 & b_0 & \\
\hline
 & s_N & s_{N-1} & s_{N-2} & \dots & s_1 & s_0 &
\end{array}
$$

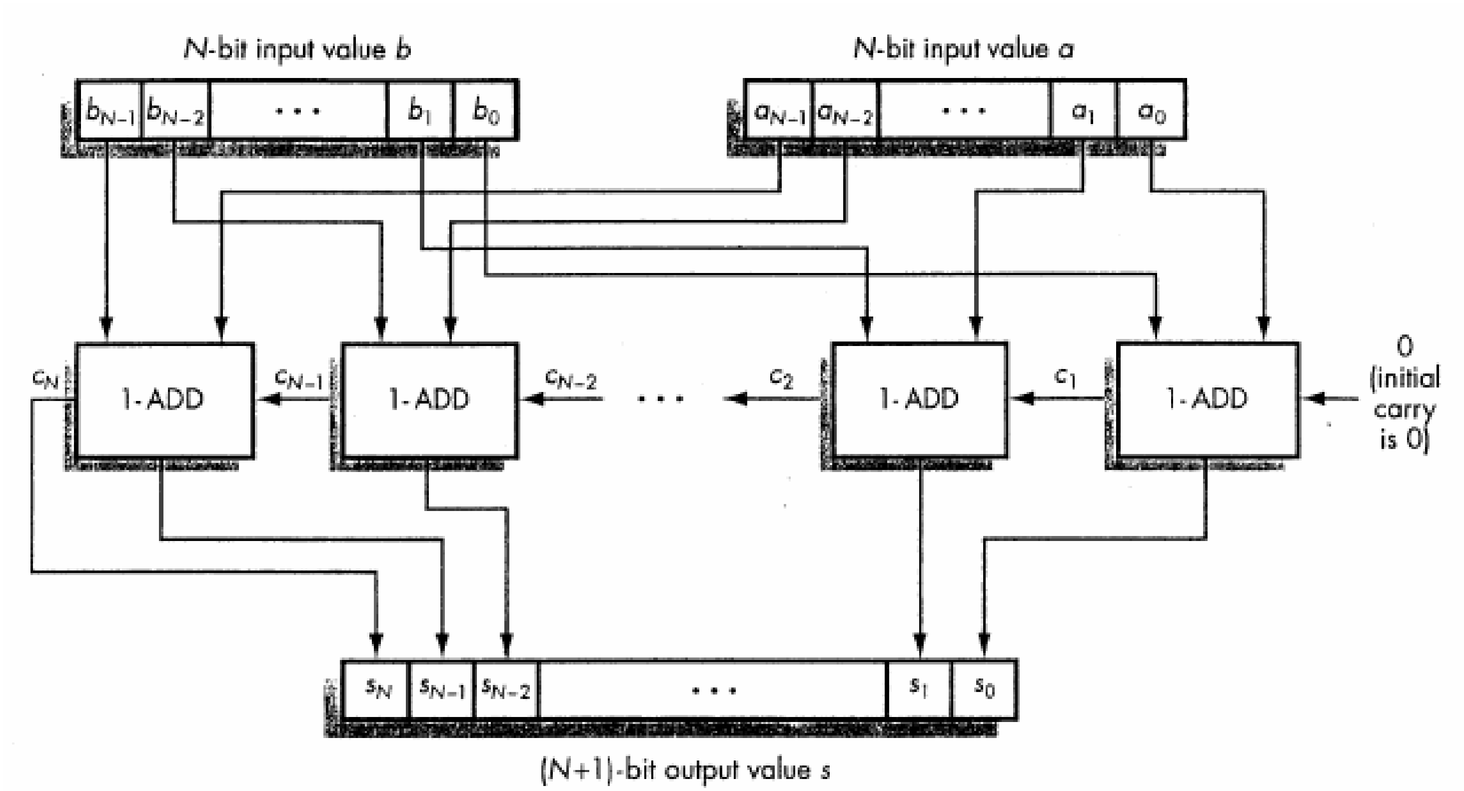
Need *N* 1-bit adders

1-bit adder



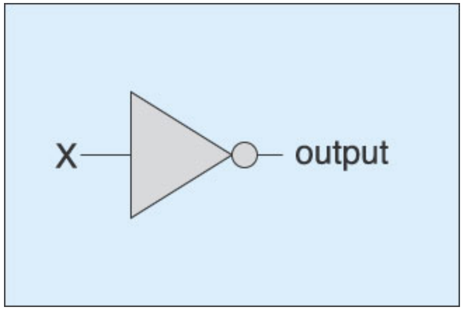
Do yourself: Write truth table, circuit.

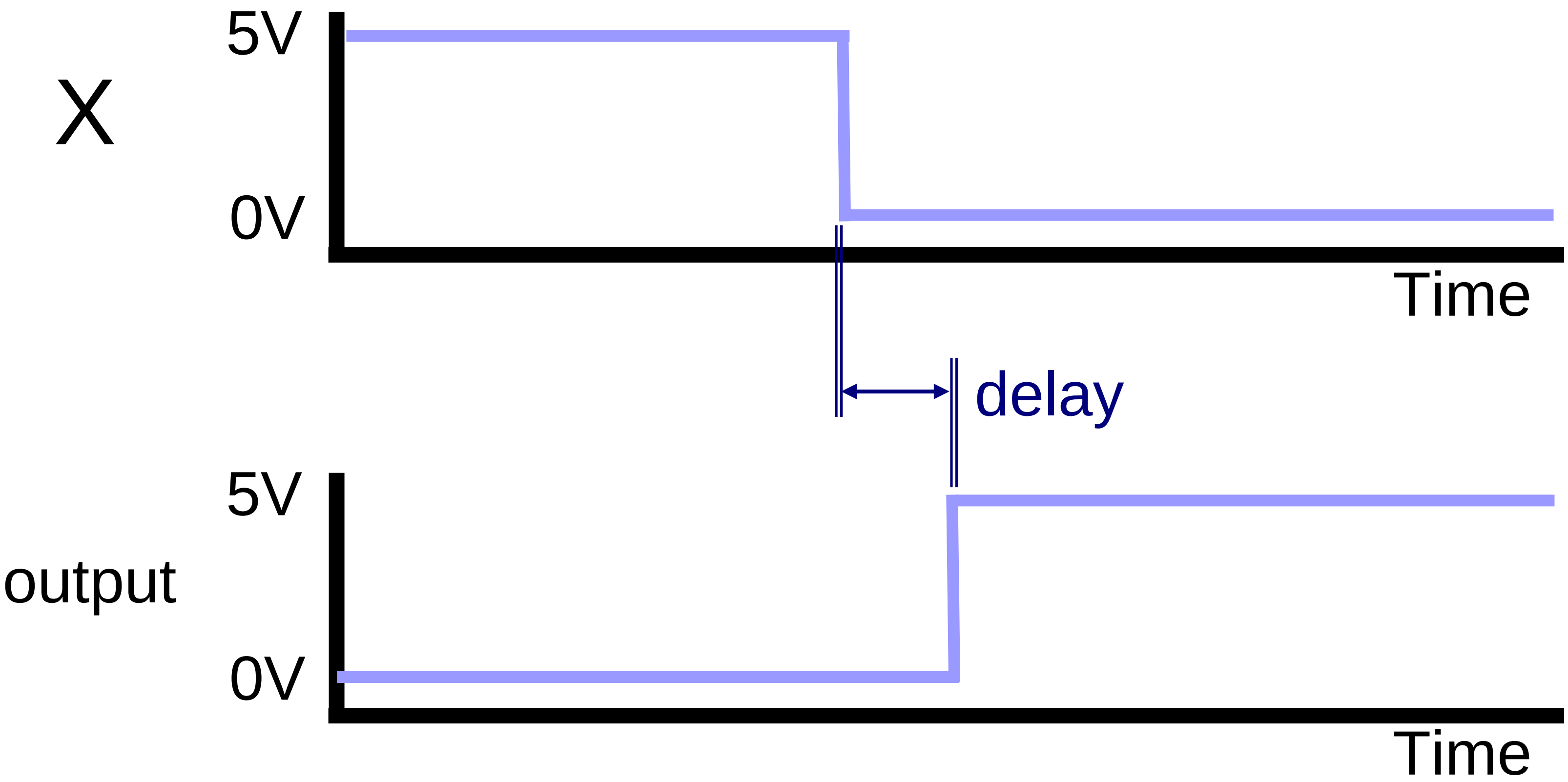
A Full Adder (from handout)



Timing Diagram

NOT gate

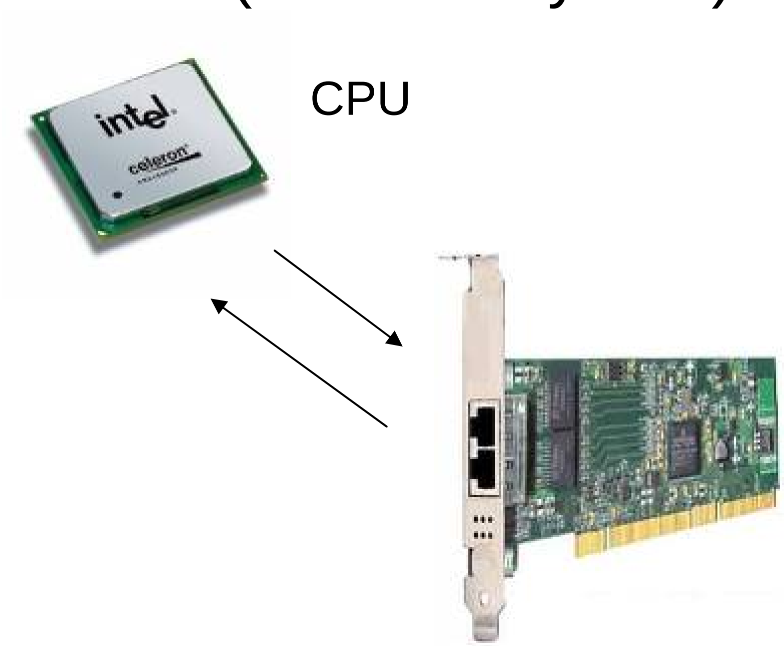




Memory

Going beyond combinational circuits

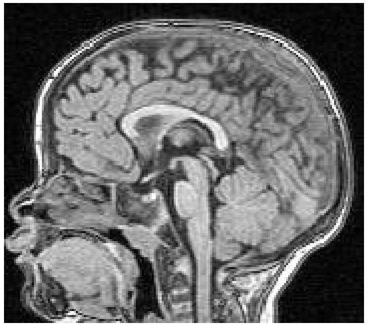
- Need 2-way communication between circuits (i.e. need cycles!)
- Need memory (scratchpad)



CPU

Ethernet card

What do you understand by ‘memory”?

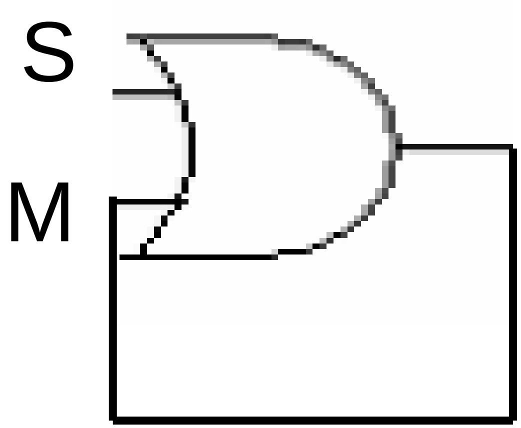


How can you tell that a 1-year old child has it?

Behaviorist’s answer: His/her actions depend upon past events.

Matt likes Sue but he doesn’t like changing his mind

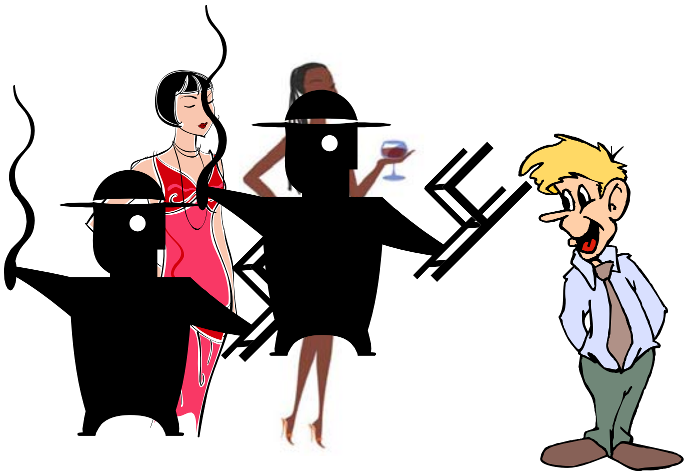
- Represent with a circuit: Matt will go to the party if Sue goes or if he already wanted to go

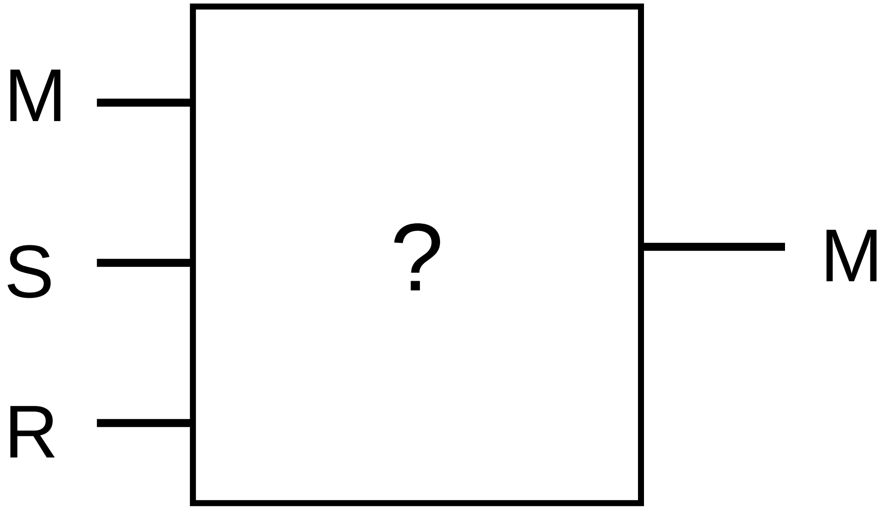


Is this well-defined?

Enter Rita

- Matt will go to the party if Sue goes OR if the following holds: if Rita does not go *and* he already wanted to go.

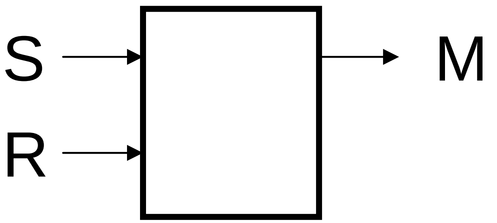


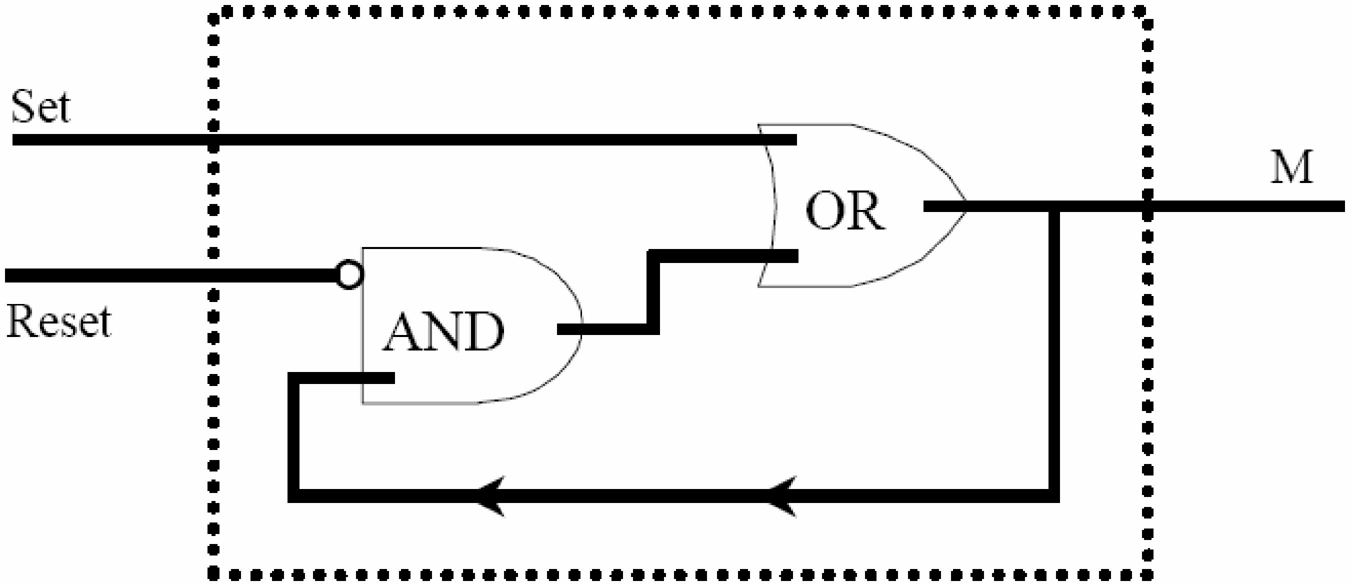


R, S: "**control**" inputs

What combination of R, S changes M?

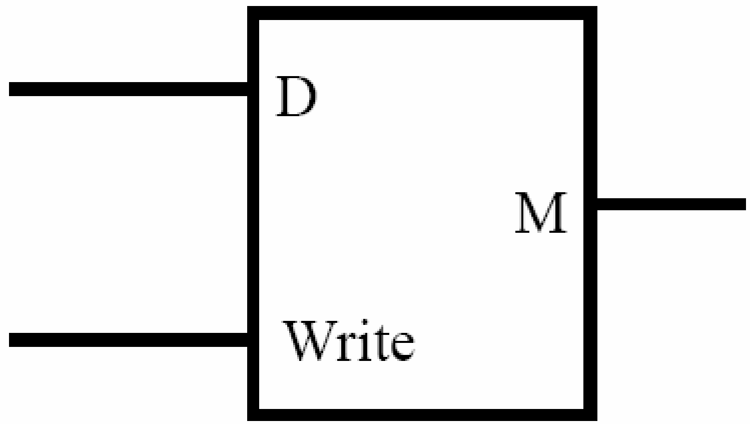
Flip-Flop





- M becomes 1 if Set is turned on
- M becomes 0 if Reset is turned on
- Otherwise (if both are 0), M just remembers its value

A more convenient form of memory

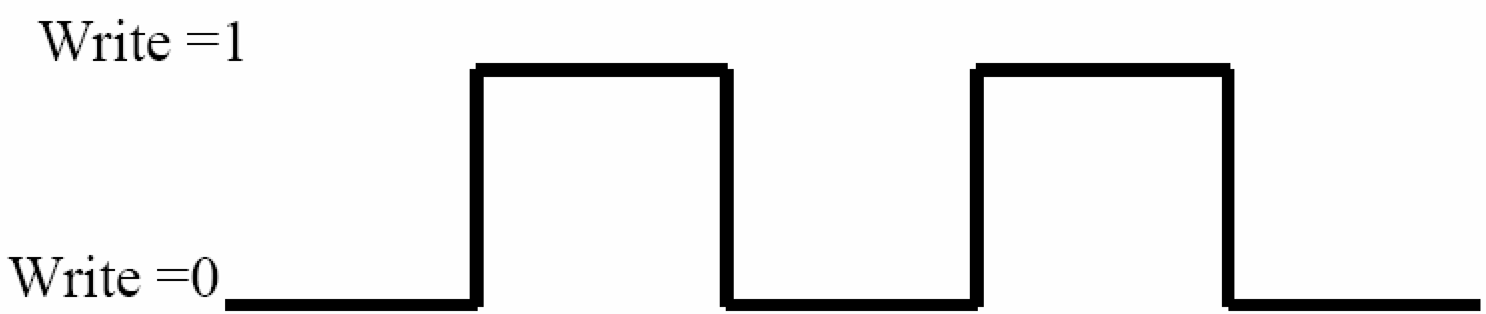


- If Write = 0, M just keeps its value. (It ignores D.)
- If Write = 1, then M becomes set to D

"Data Flip-Flop" or "D flip flop."

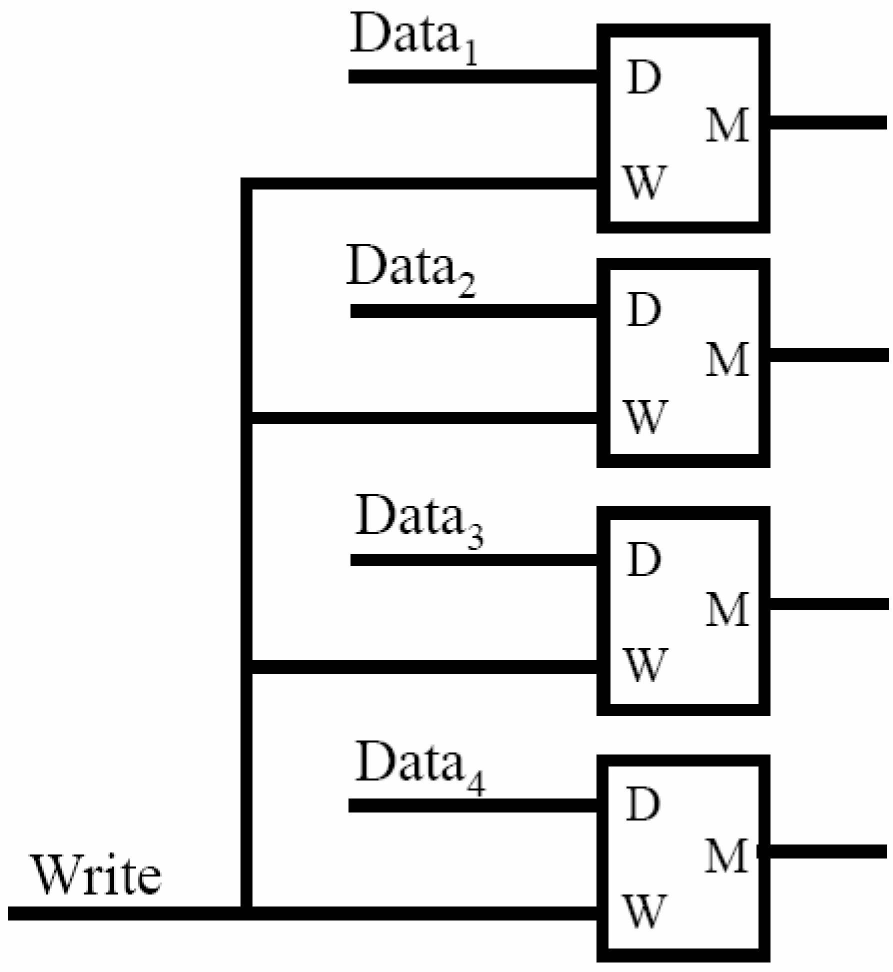
What controls the “Write” signal?

- Often, the system clock!
- “clock” = device that sends out a fluctuating voltage signal that looks like this



“Computer speed” often refers to the clock frequency (e.g. 2.4GHz)

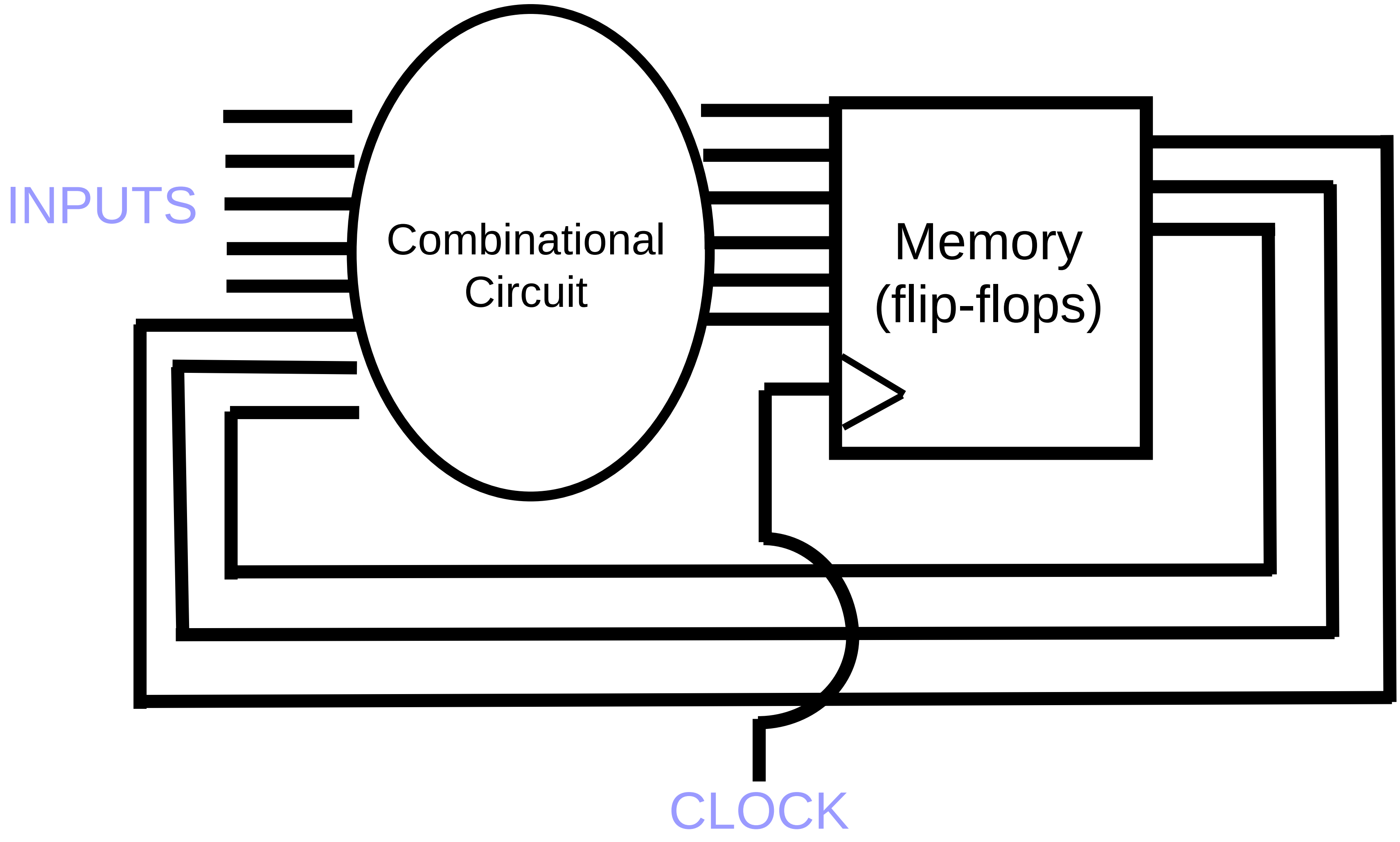
Memory “Register”: 4 bits



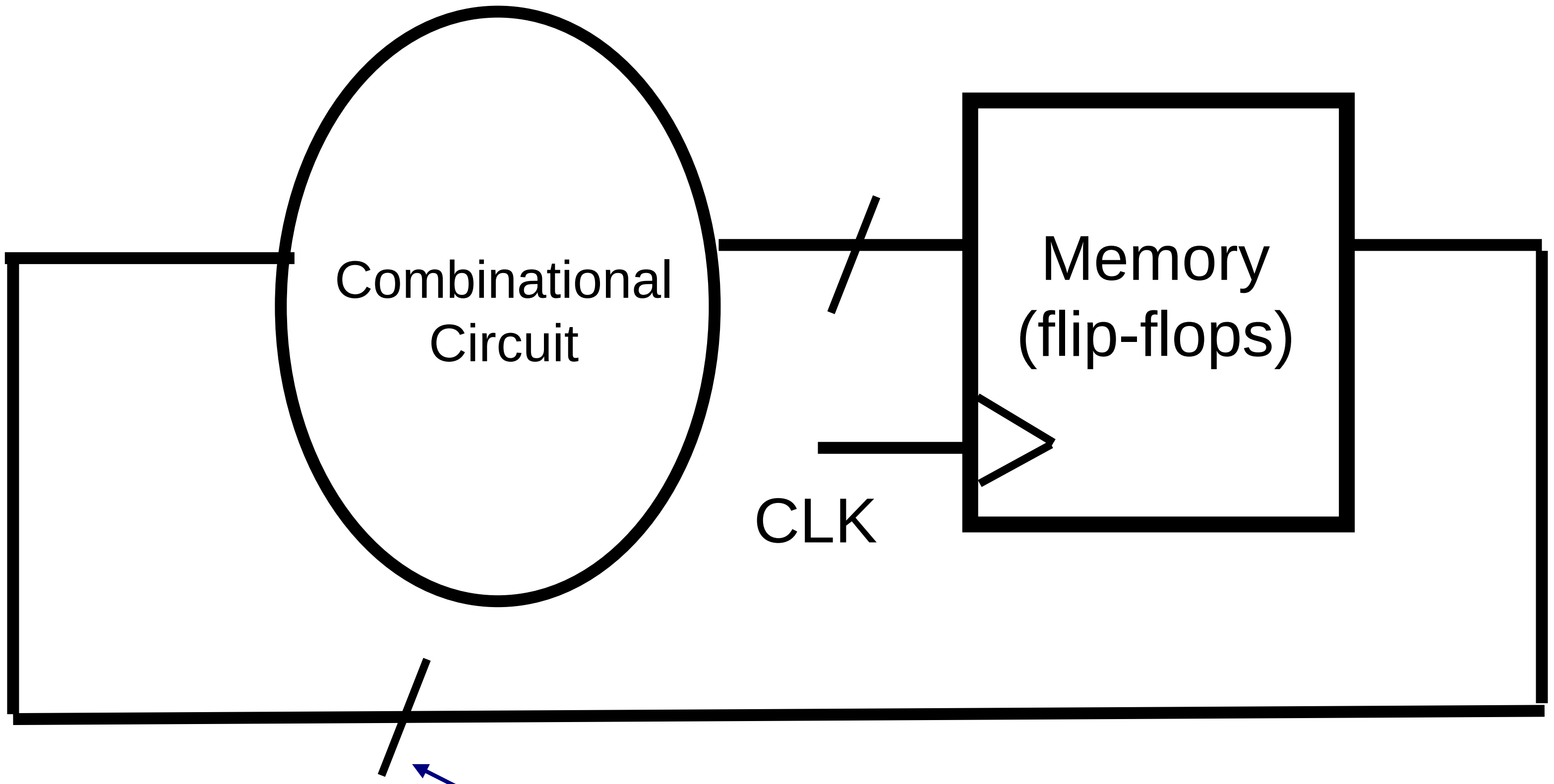
Clocked Sequential Circuits

Synchronous Sequential Circuit

(aka Clocked Sequential Circuit)



Shorthand



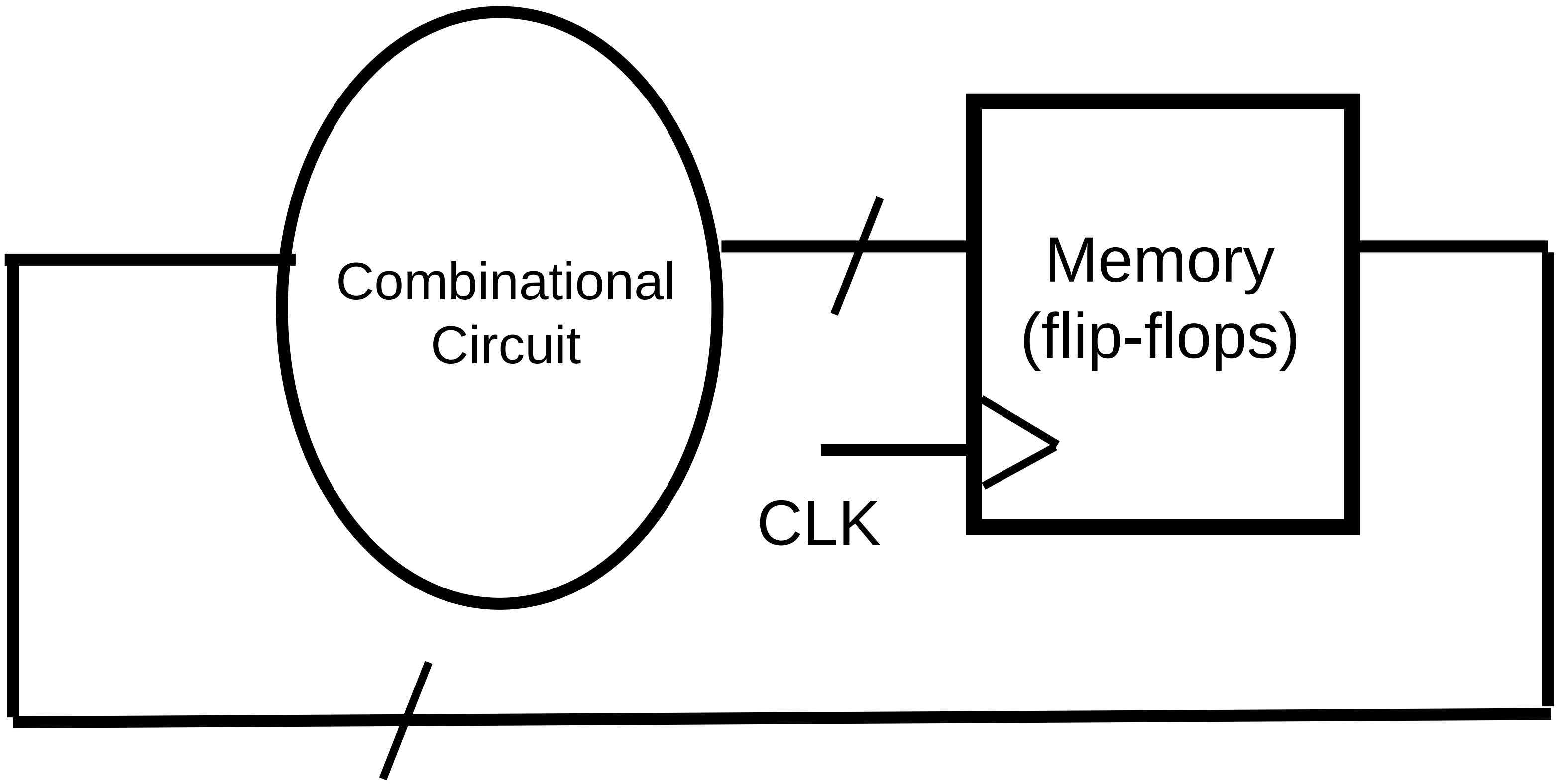
This stands for “lots of wires”

Clock Speeds

1974	Intel 8080	2 MHz (Mega = Million)
1981	Original IBM PC	4.77 MHz
1993	Intel Pentium	66 MHz
2005	Pentium 4	3.4 GHz (Giga = Billion)

Heinrich Hertz
1857-94

What limits clock speed?



Delays in combinational logic (remember the adder)

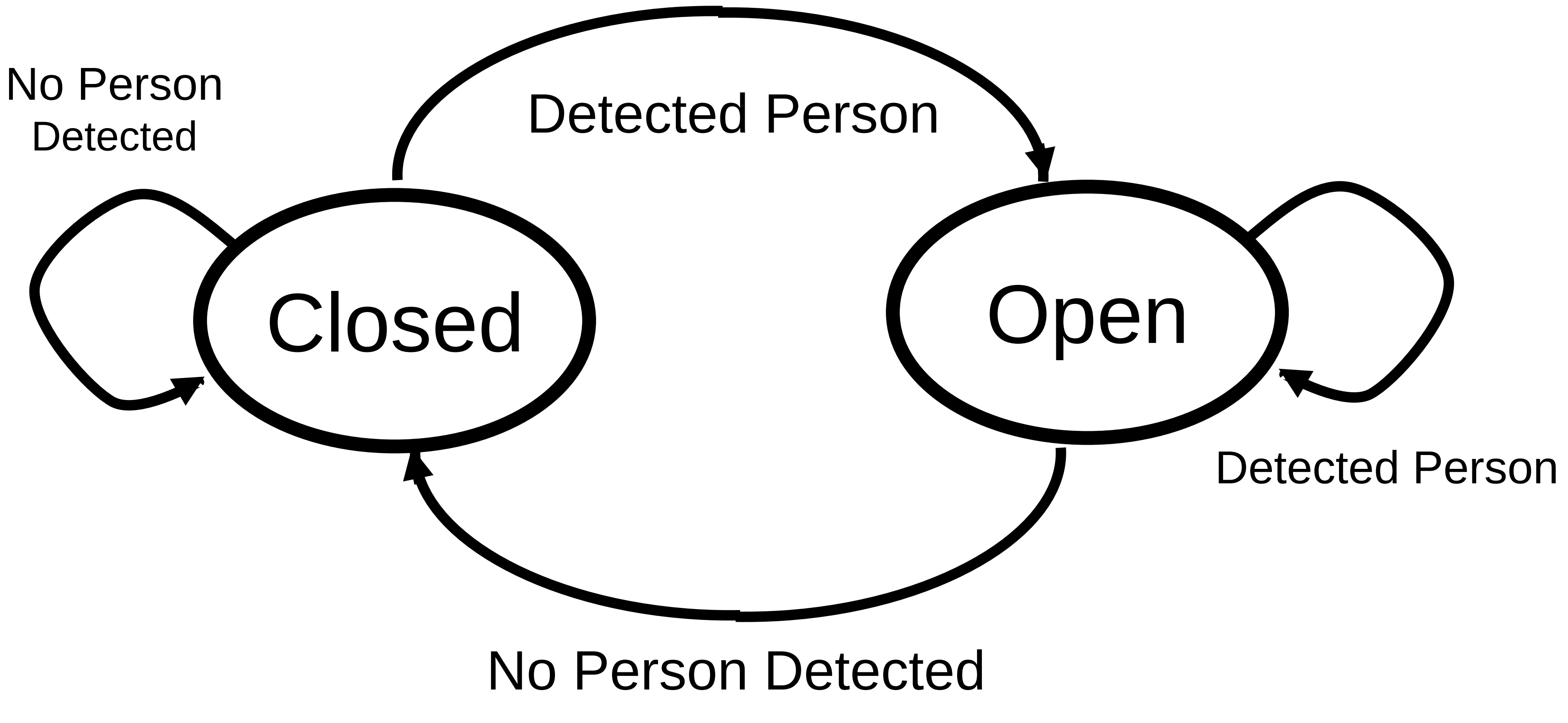
During 1 clock cycle of Pentium 4, light travels: **4 inches**

Sequential Circuits (Recap.)

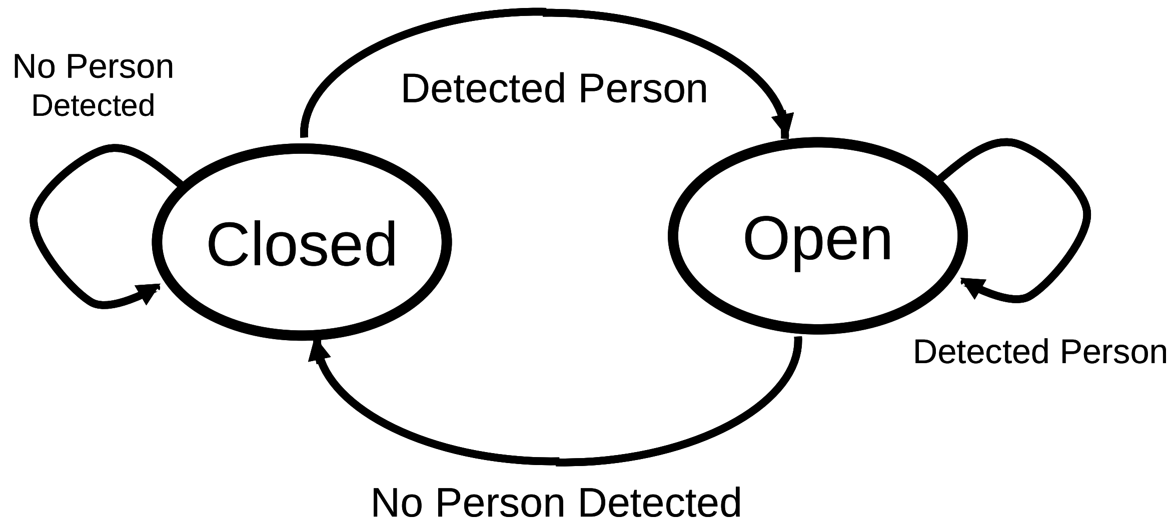
- Circuits with AND, OR and NOT gates.
- Cycles ***are*** allowed.
- Can exhibit “memory”.

Finite State Machines

State diagram for automatic door



Implementing as synchronous circuit



INPUT

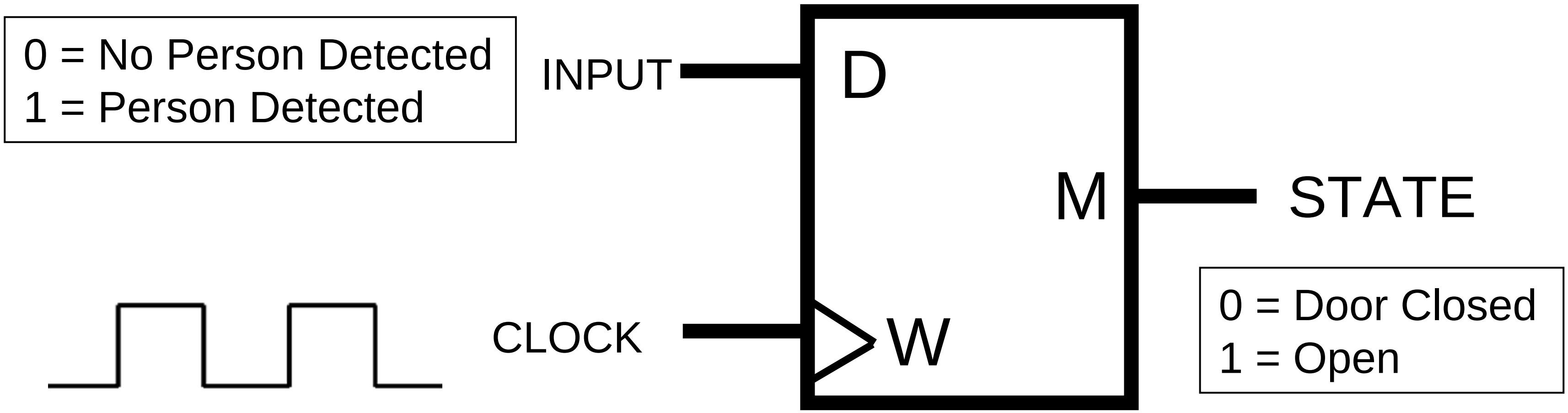
0 = No Person Detected
1 = Person Detected

STATE

0 = Door Closed
1 = Open

Input	Present State	Next State
0	0	0
1	0	1
0	1	0
1	1	1

Implementation



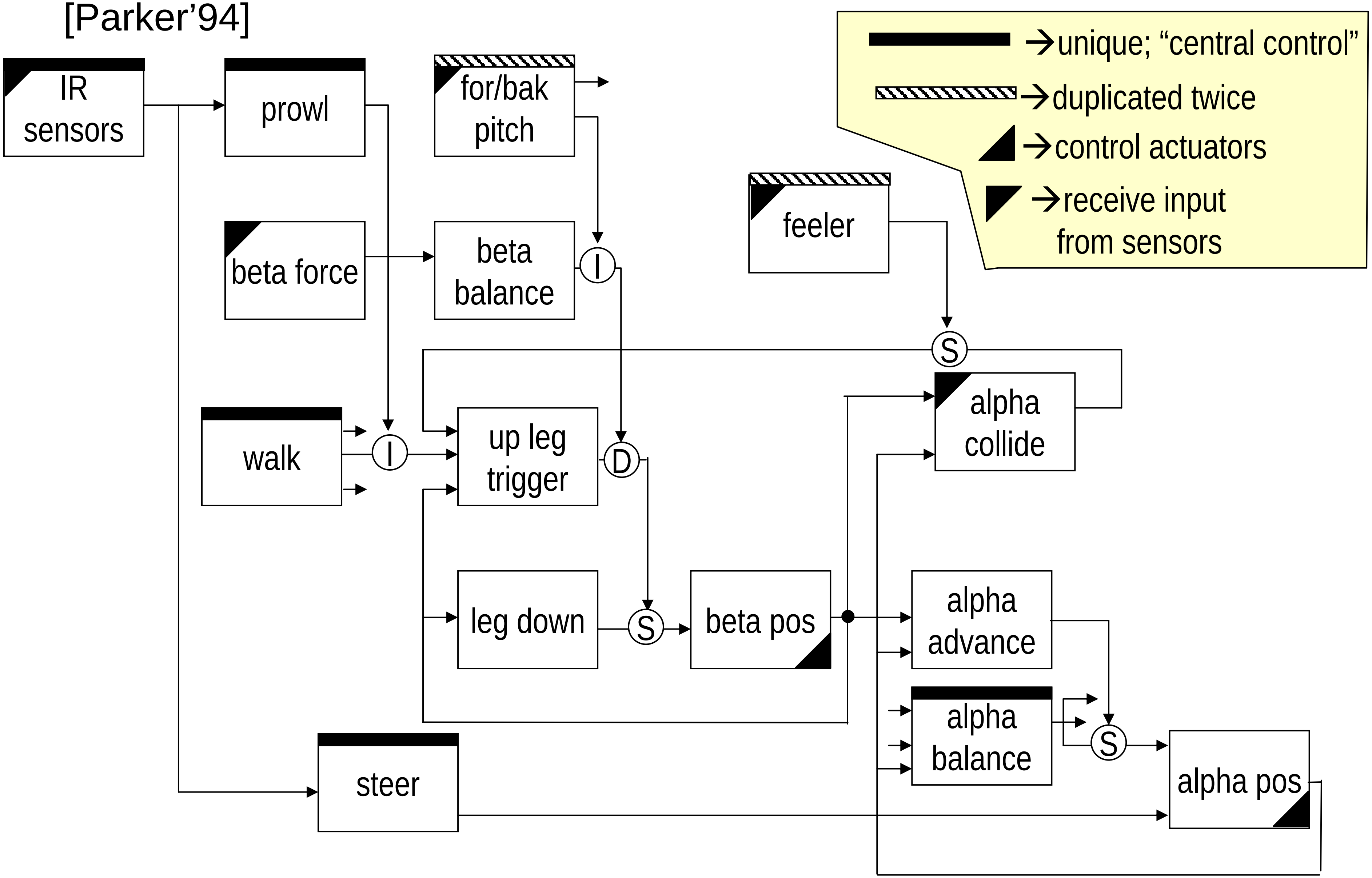
Other examples of FSMs

- Sisyphus

- Brook’s Genghis (51 FSMs) (see p. 46 in our text)
- Human Soul a la Aquinas (see Handout)

Portion of Genghis AFSM Network

[Parker'94]



Next time...

- How computers execute programs.
- Discuss Boole/Clarke “proof” of the existence of God.