Memory; Sequential & Clocked Circuits; Finite State Machines

COS 116, Spring 2012

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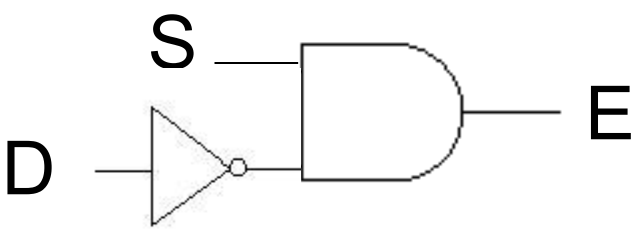
Recap: Boolean Logic

Boolean Expression $E = S \text{ AND } \overline{D}$

Boolean Circuit



Truth table:

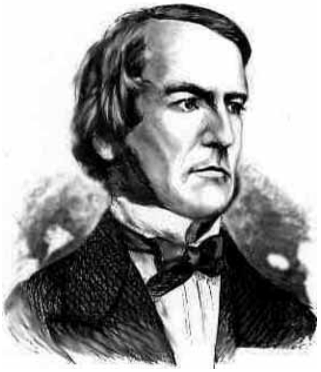
Value of E for every possible D, S.

TRUE=1; FALSE= 0.

D	S	E
0	0	0
0	1	1
1	0	0
1	1	0

Truth table has 2^k rows if the number of variables is k

Boole’s reworking of Clarke’s “proof” of existence of God (see handout – after midterm)



- General idea: Try to prove that Boolean expressions $E_1, E_2, \ldots, E_k$ cannot simultaneously be true
- Method: Show $E_1 \cdot E_2 \cdot \ldots \cdot E_k = 0$
- Discussion for after Break: What exactly does Clarke’s “proof” prove? How convincing is such a proof to you?

Also: Do Google search for “Proof of God’s Existence.”

Circuit for binary addition?

25	11001
+ 29	11101
54	110110

Want to design a circuit to add any two *N*-bit integers.

Q: Is the truth table method useful for N=64?

Modular design for N-bit adder

$$\begin{array}{rcccccc} & & c_{N-1} & c_{N-2} & \dots & c_1 & c_0 \\ & & a_{N-1} & a_{N-2} & \dots & a_1 & a_0 \\ + & & b_{N-1} & b_{N-2} & \dots & b_1 & b_0 \\ \hline & s_N & s_{N-1} & s_{N-2} & \dots & s_1 & s_0 \end{array}$$

Carry bits

Suffices to use *N* 1-bit adders!

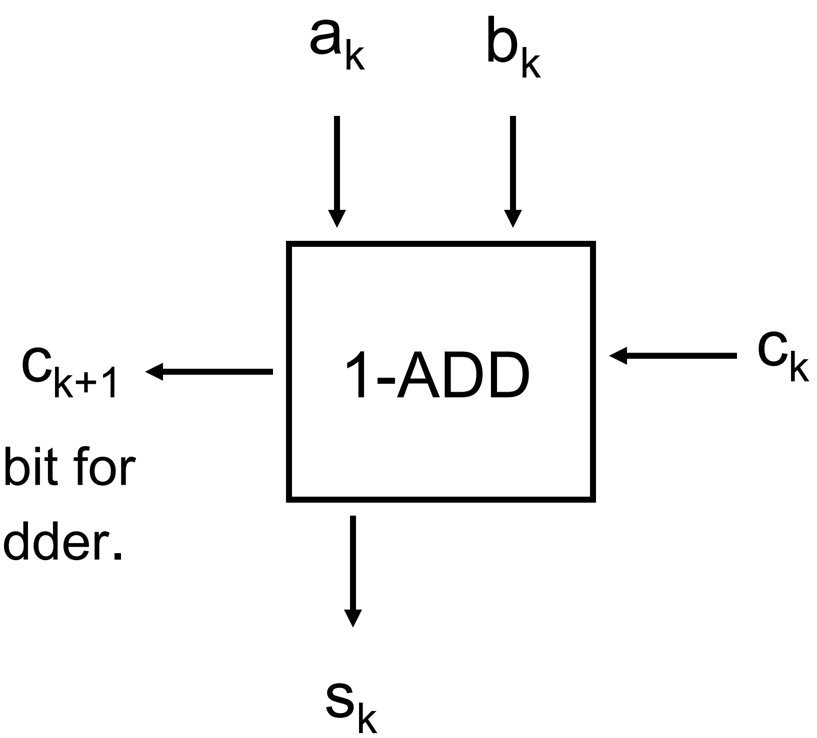
Modular design

Have small number
of basic components.

Put them together to achieve
desired functionality

Basic principle of modern industrial design;
recurring theme in next few lectures.

1-bit adder

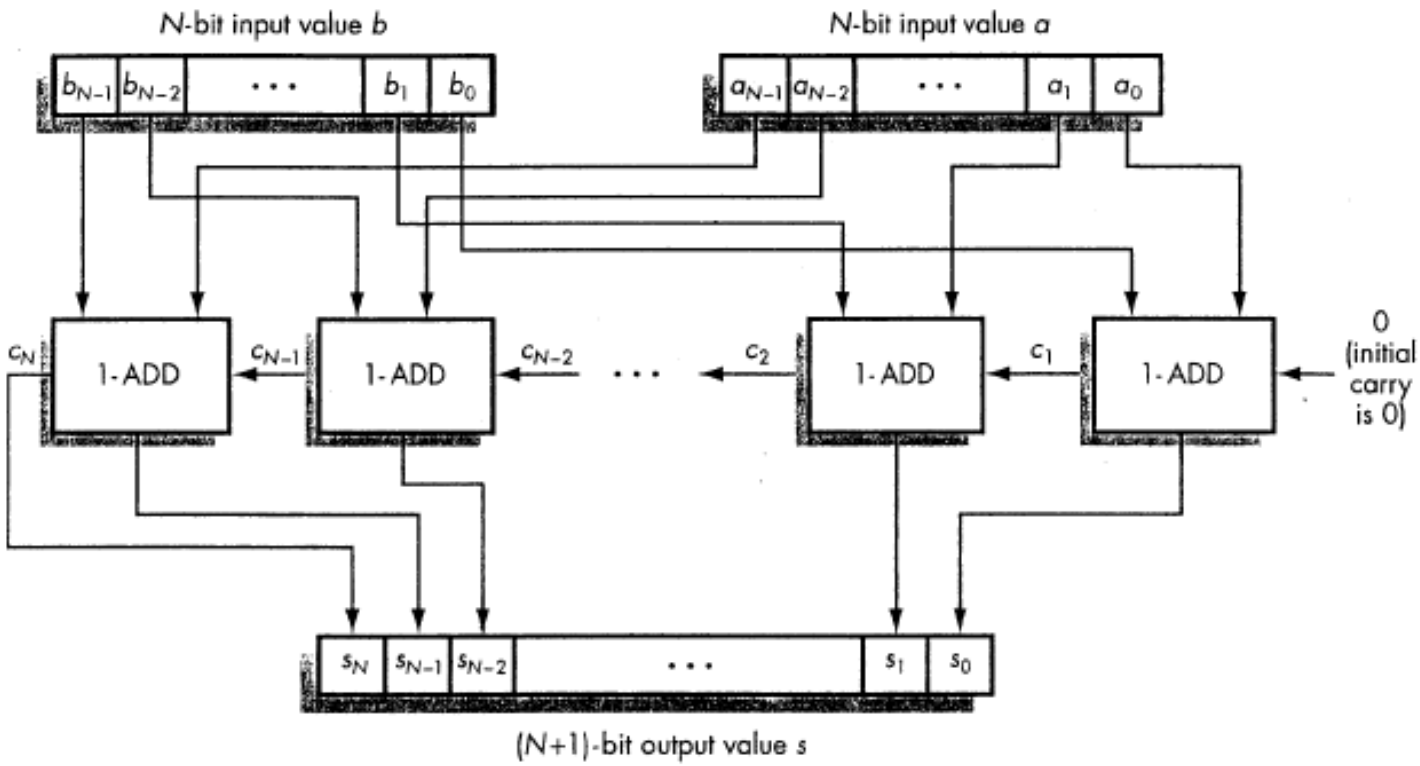


(Carry from previous adder)

Carry bit for next adder.

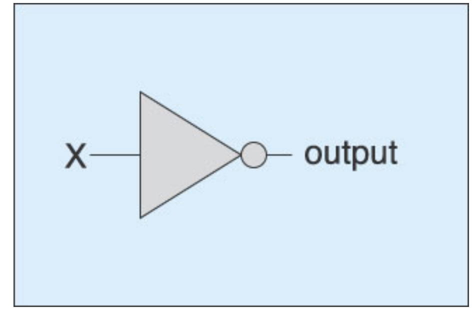
Do yourself: Write truth table, circuit.

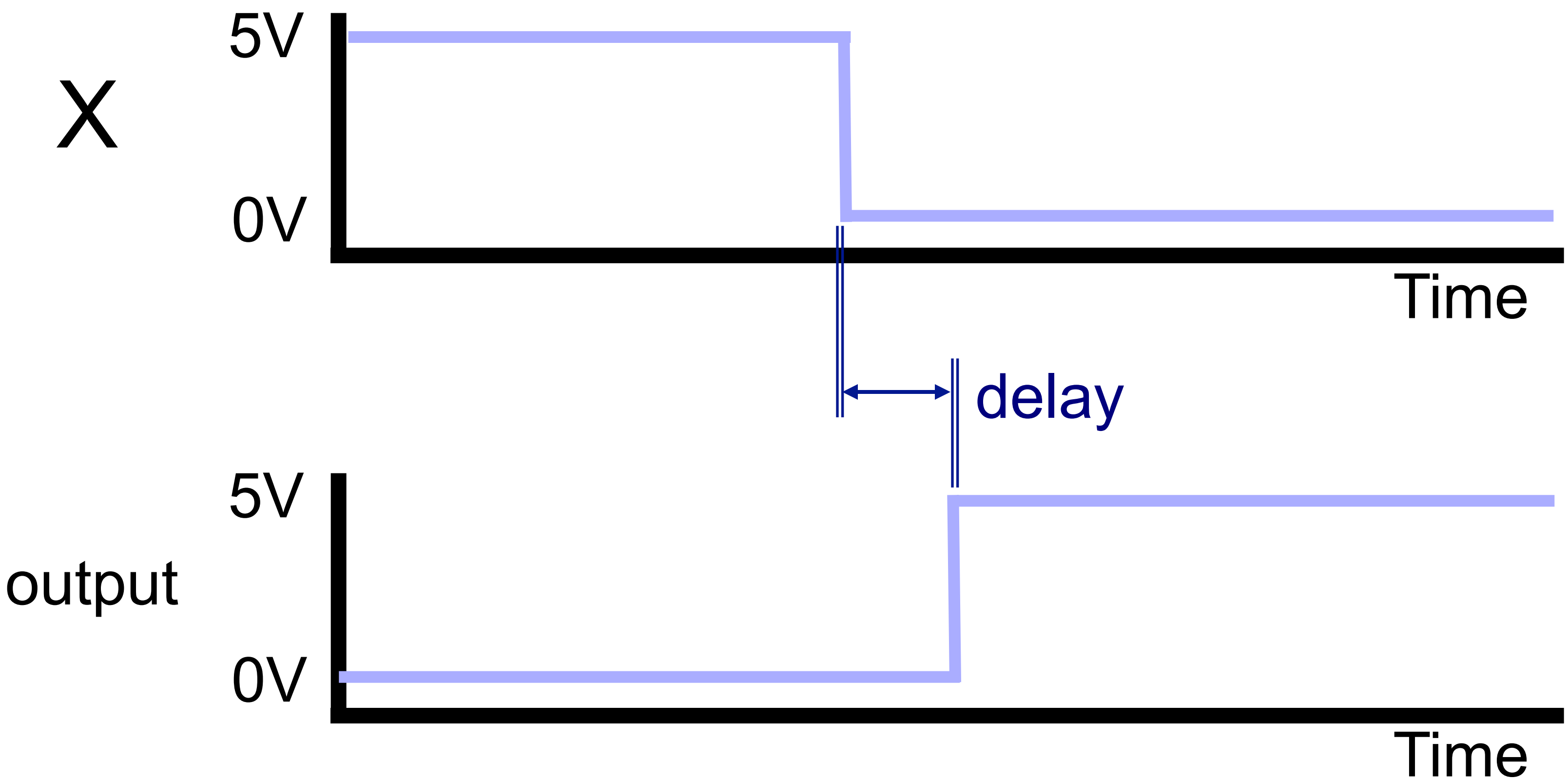
A Full Adder (see logic reading)



Timing Diagram

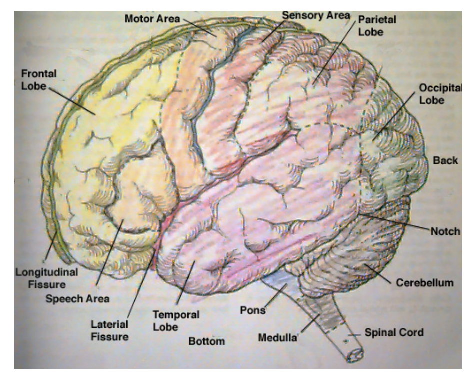
NOT gate





Memory

Rest of this lecture:
How boolean circuits have “memory”.



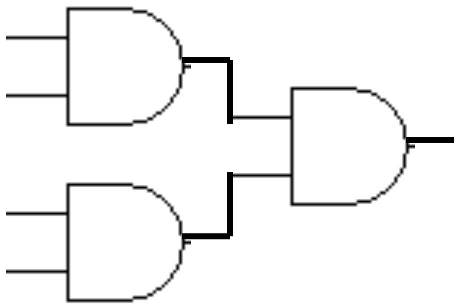
What do you understand by ‘memory’…?

How can you tell that a 1-year old child has it?

Behaviorist’s answer: Child’s actions depend upon past events.

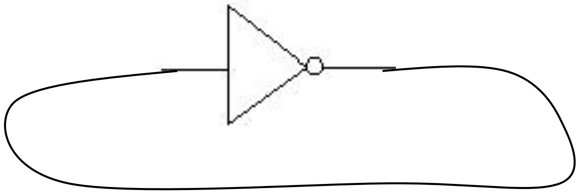
Combinational circuit

- Boolean gates connected by wires



Wires: transmit voltage
(and hence value)

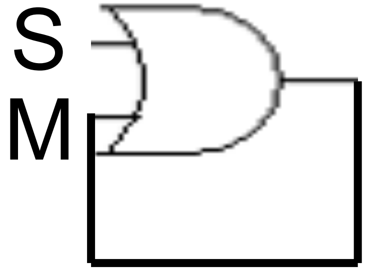
- Important: no cycles allowed



Today: Circuits with loops; aka "Sequential Circuits"

Matt likes Sue but he doesn't like changing his mind

- Represent with a circuit: Matt will go to the party if Sue goes or if he already wanted to go



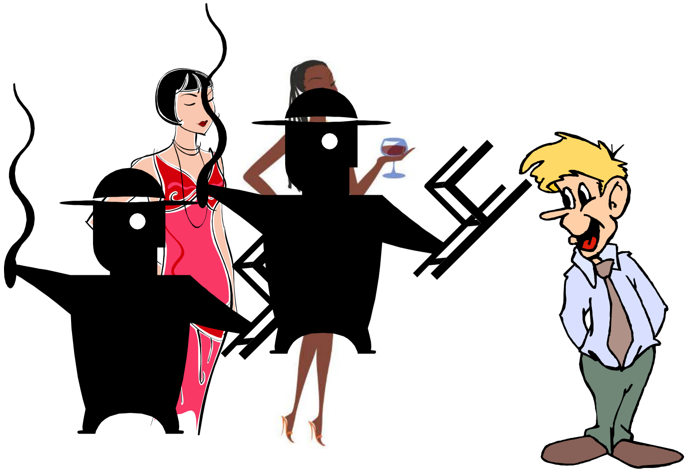
Is this well-behaved?!?

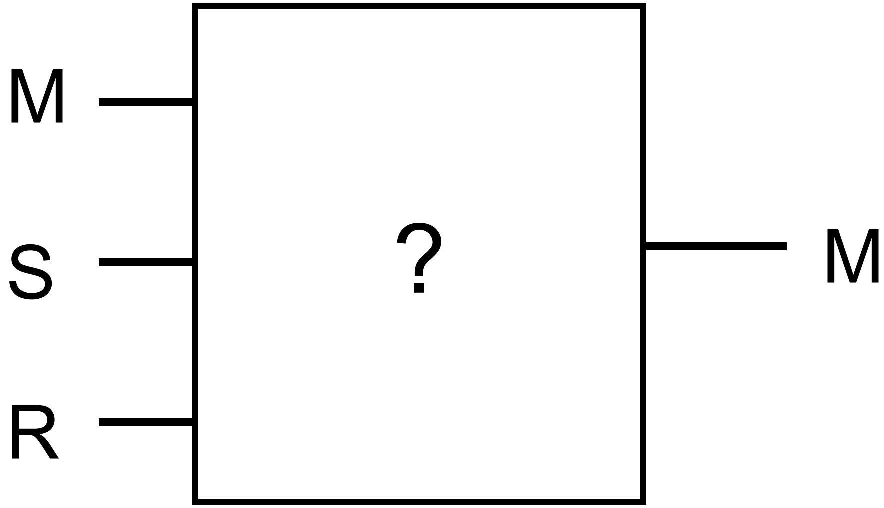
Sequential Circuits

- Circuits with AND, OR and NOT gates.
- Cycles ***are*** allowed (ie outputs can feed back into inputs)
- Can exhibit "memory".
- Sometimes may have "undefined" values

Enter Rita

- Matt will go to the party if Sue goes OR if the following holds: if Rita does not go *and* he already wanted to go.

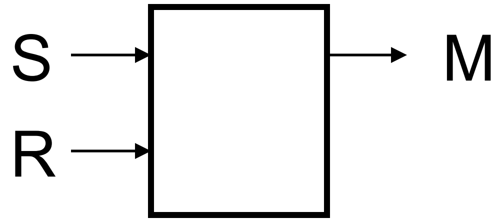


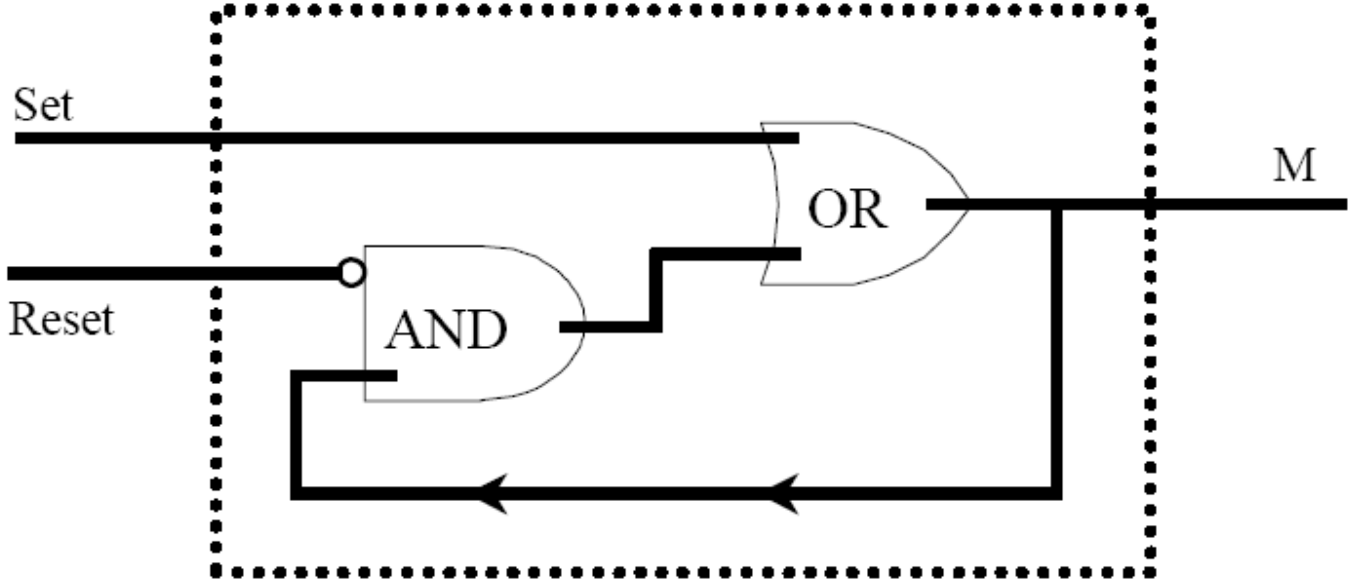


R, S: "**control**" inputs

What combination of R, S changes M?

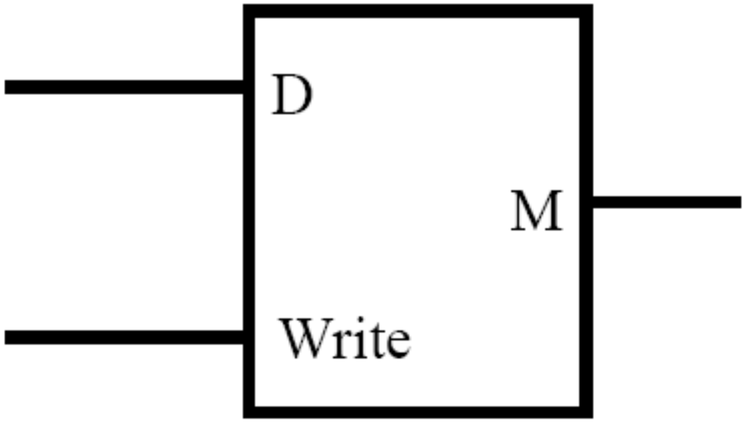
R-S Flip-Flop





- M becomes 1 if Set is turned on
- M becomes 0 if Reset is turned on
- Otherwise (if both are 0), M just remembers its value

A more convenient form of memory

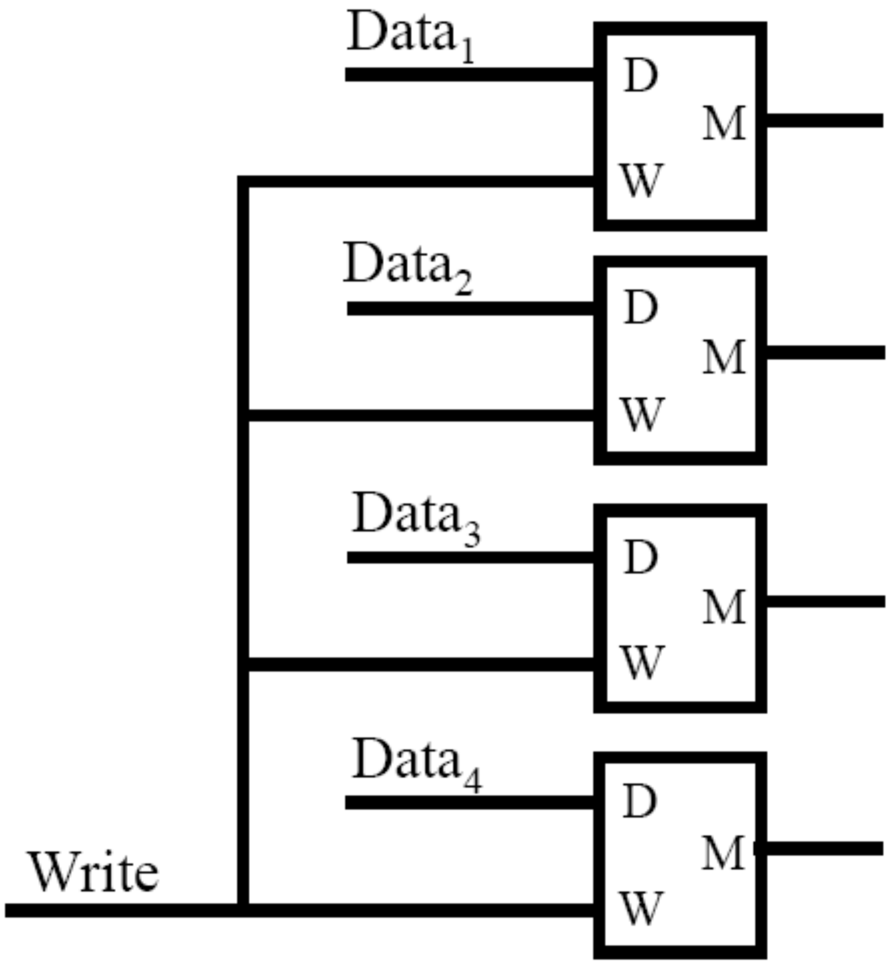


No "undefined" outputs ever!

- If Write = 0, M just keeps its value. (It ignores D.)
- If Write = 1, then M becomes set to D

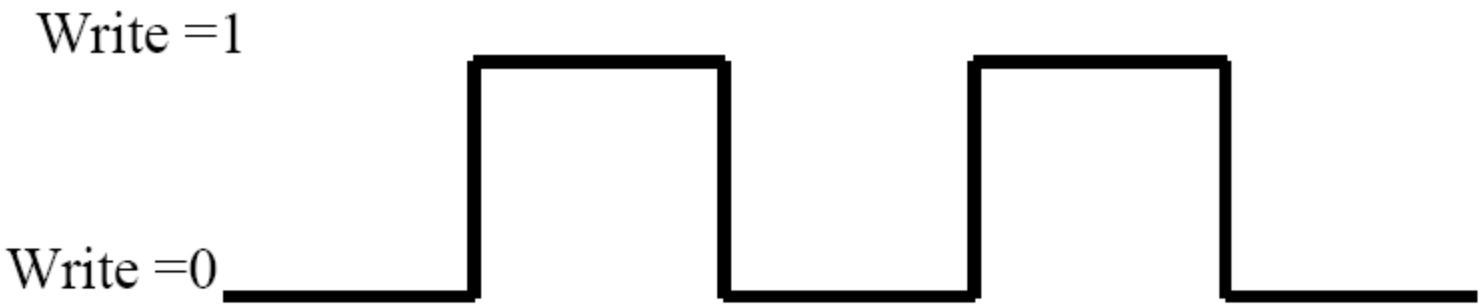
Fact: "Data Flip-Flop" (or "D flip flop") can be created using R-S flip flops!

Register with 4 bits of memory



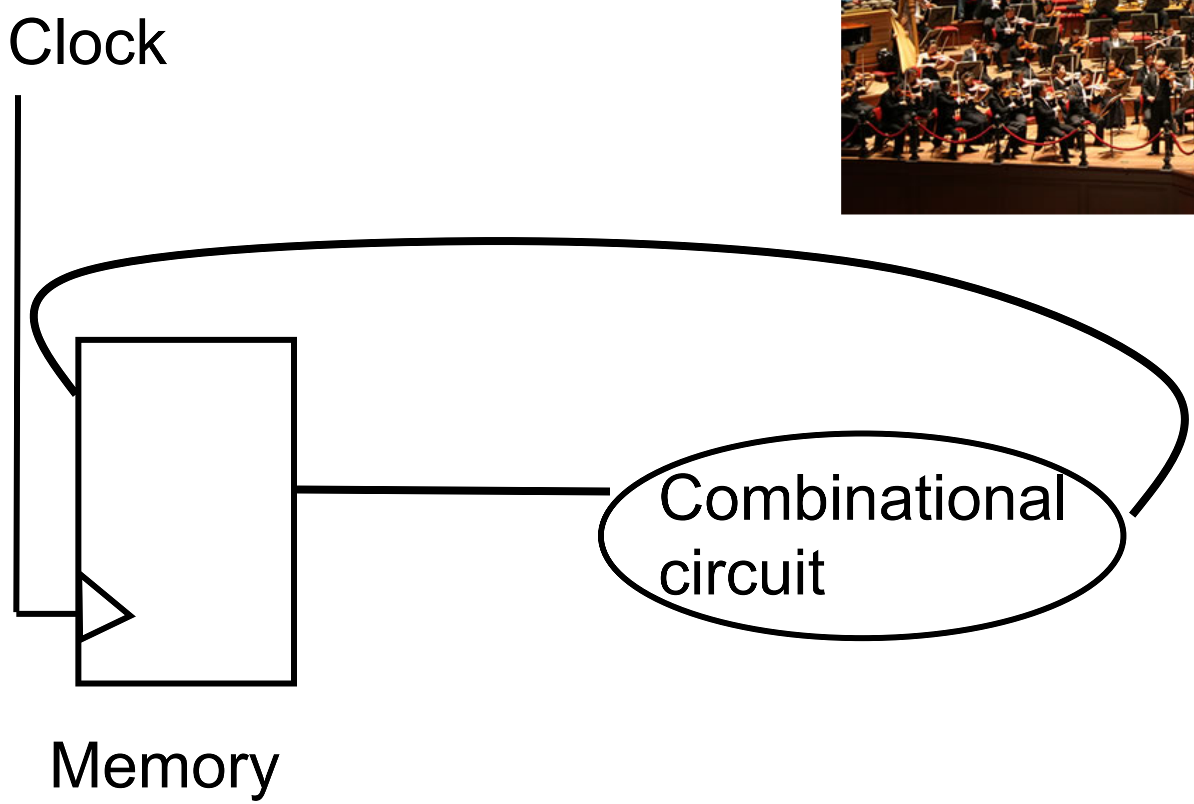
What controls the "Write" signal?

- Often, the system clock!
- "clock" = device that sends out a fluctuating voltage signal that looks like this



"Computer speed" often refers to the clock frequency (e.g. 2.4GHz)

The “symphony” inside a computer

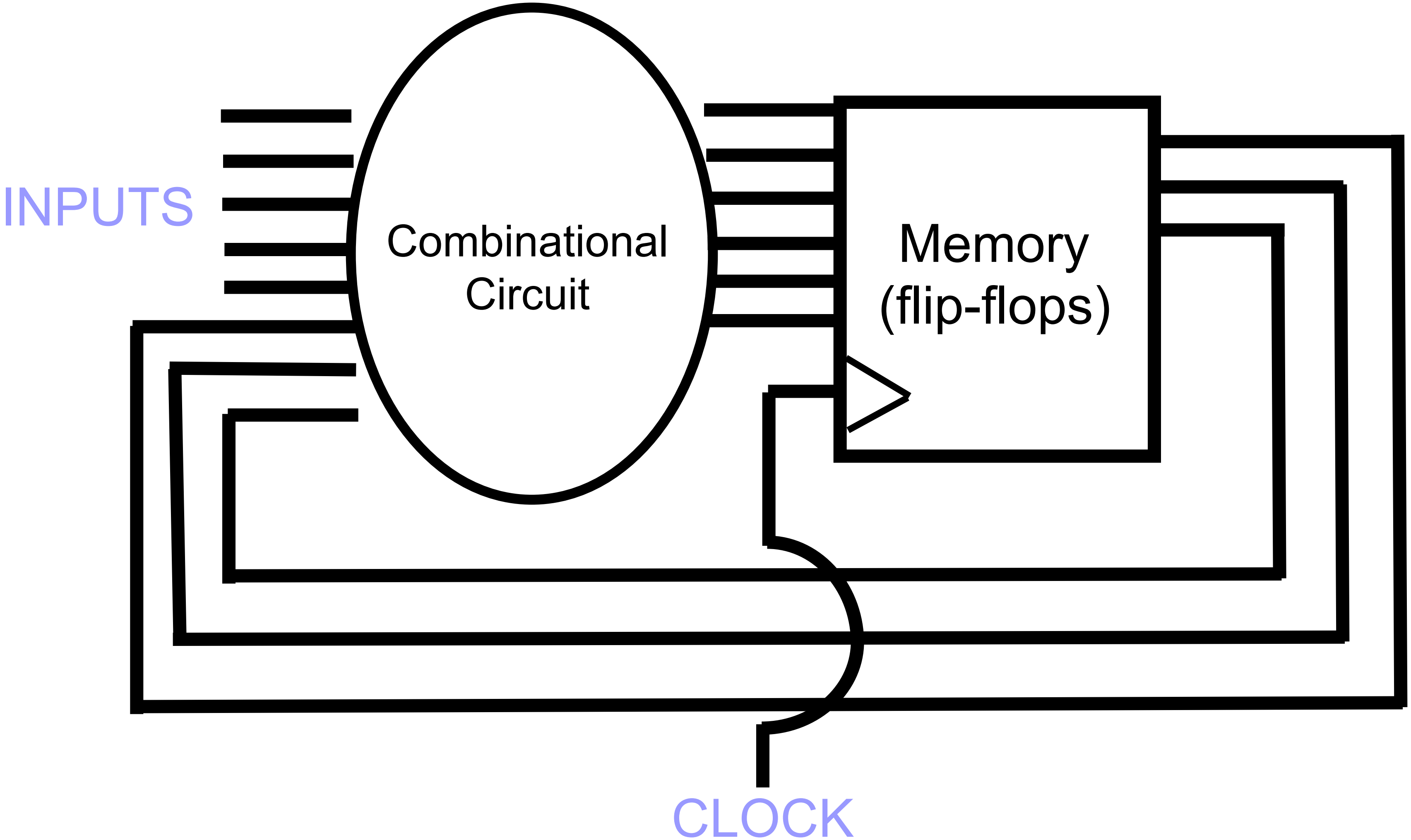


Clocked Sequential Circuit (aka Synchronous Circuits)

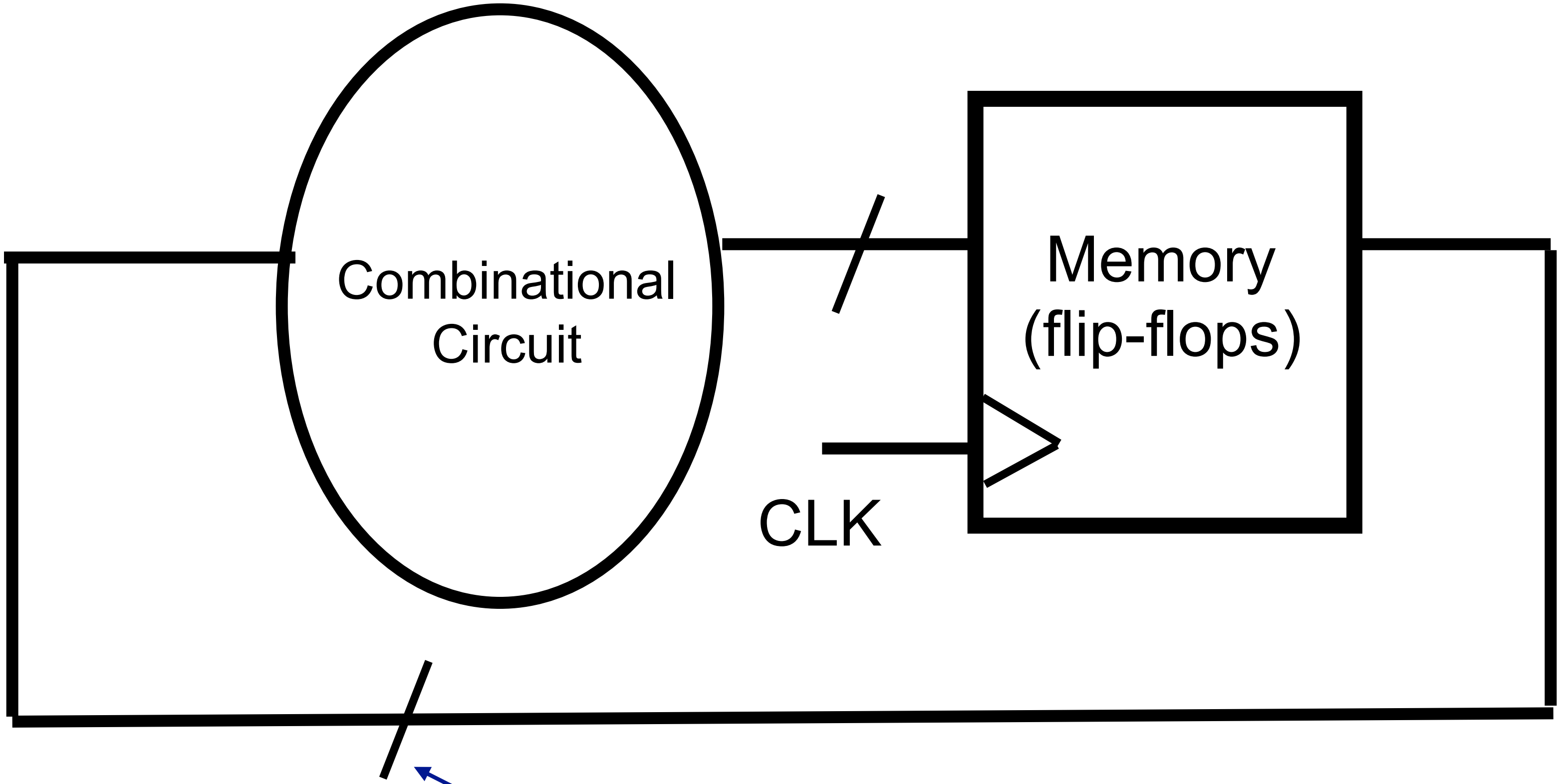
Clocked Sequential Circuits

Synchronous Sequential Circuit

(aka Clocked Sequential Circuit)



Shorthand



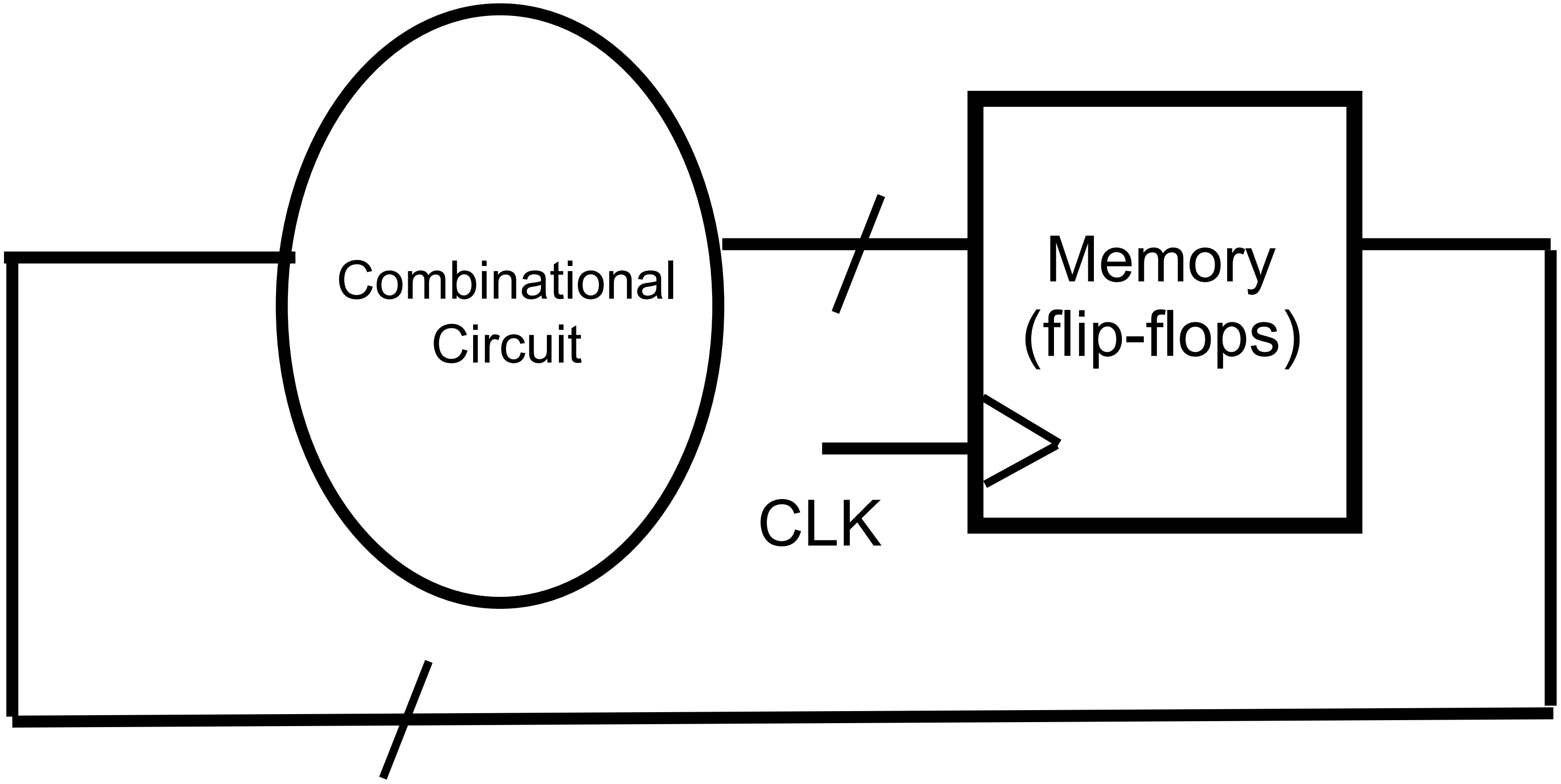
This stands for “lots of wires”

Clock Speeds

Heinrich Hertz
1857-94

1974	Intel 8080	2 MHz (Mega = Million)
1981	Original IBM PC	4.77 MHz
1993	Intel Pentium	66 MHz
2005	Pentium 4	3.4 GHz (Giga = Billion)

What limits clock speed?



Delays in combinational logic (remember the adder)

During 1 clock cycle of Pentium 4, light travels: **4 inches**

Next lecture….

Finite State Machines

Example: State diagram for automatic door at grocery store