|       |           | 24.00 | -               |             |    | _          | -  |          | - | - |   | _ | 10.0 |
|-------|-----------|-------|-----------------|-------------|----|------------|----|----------|---|---|---|---|------|
| 使是五   |           |       |                 | -           |    |            | 群  | 鞋        | 벖 | 锐 |   | 群 | -    |
| 使是些证  | 南南南南      | 4     | 쳐뀱              |             | F  |            | 群  | 뢦        | 뢦 | 뢦 |   | 群 | *    |
| 使是些证  |           |       |                 |             |    | 봾          | 群  | 뿺        | 뢦 | 虹 | F | 볛 | 社    |
| 使甚些致  |           |       |                 |             |    |            | 벖  | 群        | 벖 | 뢠 | ſ | 群 | 4    |
| 支払    | ·<br>최퇴퇴퇴 | ₫.    | 쳐젖              |             |    | ₿<br>T     | 群  | 虹        | 뢦 | 뢦 | ſ | 群 | 林    |
| 使是些   |           |       |                 |             |    | 뿺          | 锐  | 뢦        | 벖 | 뢦 | Ľ | 斑 | *    |
| 使是些一种 |           |       |                 |             |    | 봯          | 붟- | 뢦        | 벖 | 뢦 |   | 群 |      |
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| 世世    | ·<br>최퇴퇴퇴 | ₹.    | ¥. <sub>Ң</sub> | ₿¶¥         | F  | <b>뷥</b> · | 訊- | ¥.       | 벖 | 群 |   |   | 14   |

# **Combinational Circuits**

- Q. What is a combinational circuit?

- Q. Why combinational circuits?
- A. Accurate, reliable, general purpose, fast, cheap.

#### Basic abstractions.

- On, off.
- Wire: propagates on/off value.
- Switch: controls propagation of on/off values through wires.

Applications. Cell phone, iPod, antilock brakes, microprocessors, ...

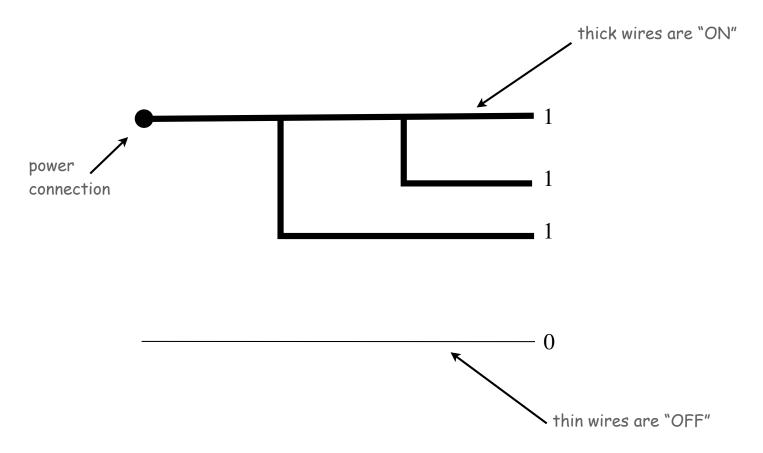


# **Building Blocks**

# Wires

#### Wires.

- ON (1): connected to power.
- OFF (0): not connected to power.
- If a wire is connected to a wire that is on, that wire is also on.
- Typical drawing convention: "flow" from top, left to bottom, right.

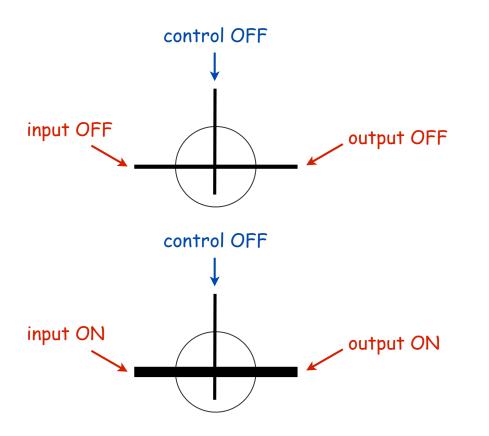


### Controlled switch.

• 3 connections: input, output, control.

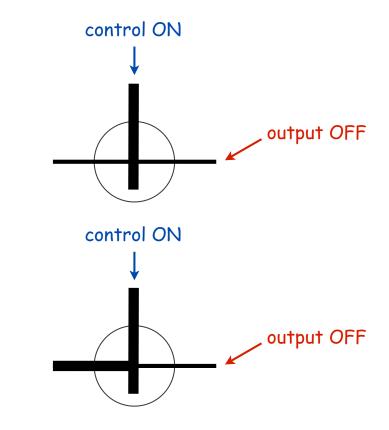
## Controlled switch.

- 3 connections: input, output, control.
- control OFF: output is connected to input



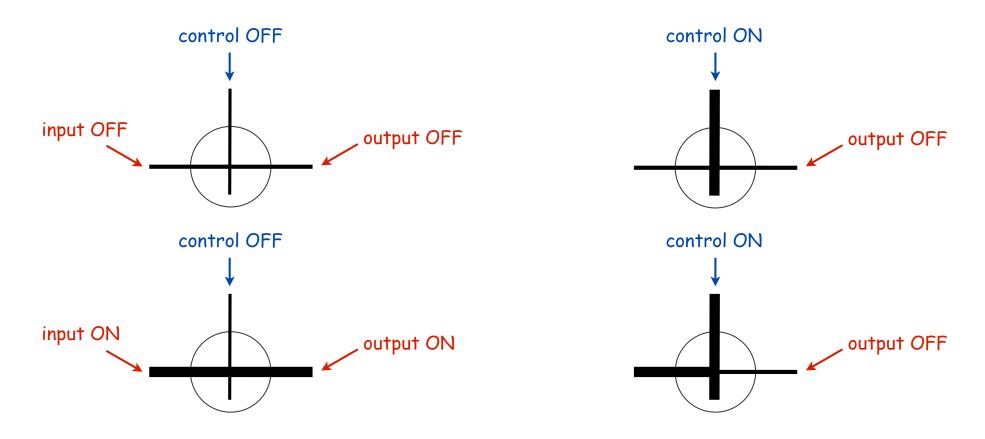
#### Controlled switch.

- 3 connections: input, output, control.
- control ON: output is disconnected from input



## Controlled switch.

- 3 connections: input, output, control.
- control OFF: output is connected to input
- control ON: output is disconnected from input

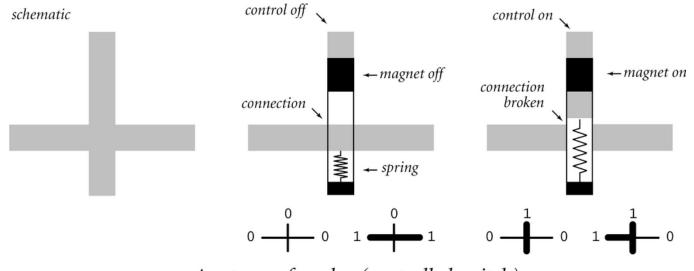


idealized model of "pass transistors" found in real integrated circuits

# Implementing a Controlled Switch

## Relay implementation.

- 3 connections: input, output, control.
- Magnetic force pulls on a contact that cuts electrical flow.



Anatomy of a relay (controlled switch)

# First Level of Abstraction

## Separates physical world from logical world.

- we assume that switches operate as specified
- that is the only assumption
- physical realization of switch is irrelevant to design

## Physical realization dictates performance

- size
- speed
- power

New technology immediately gives new computer.

Better switch? Better computer.

#### Some amusing attempts to prove the point:

| Technology | "Information"      | Switch |
|------------|--------------------|--------|
| pneumatic  | air pressure       |        |
| fluid      | water pressure     |        |
| relay      | electric potential |        |

# Controlled Switches: A First Level of Abstraction

## Real-world examples that prove the point:

| technology                              | switch |
|---|--------|
| relay                                   |        |
| vacuum tube                             |        |
| transistor                              |        |
| "pass transistor" in integrated circuit |        |
| atom-thick transistor                   | I      |

# Controlled Switches: A First Level of Abstraction?

VLSI = Very Large Scale Integration

Technology: Deposit materials on substrate.

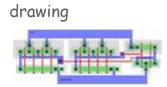
Key property: Crossing lines are controlled switches.

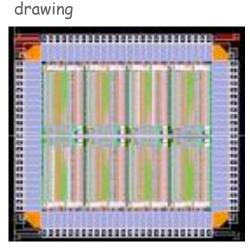
Key challenge in physical world: Fabricating physical circuits

with billions of controlled switches

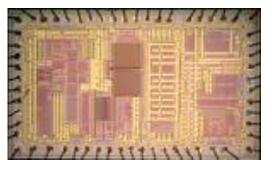
Key challenge in "abstract" world: Understanding behavior of circuits with billions of controlled switches

Bottom line: Circuit = Drawing (!)

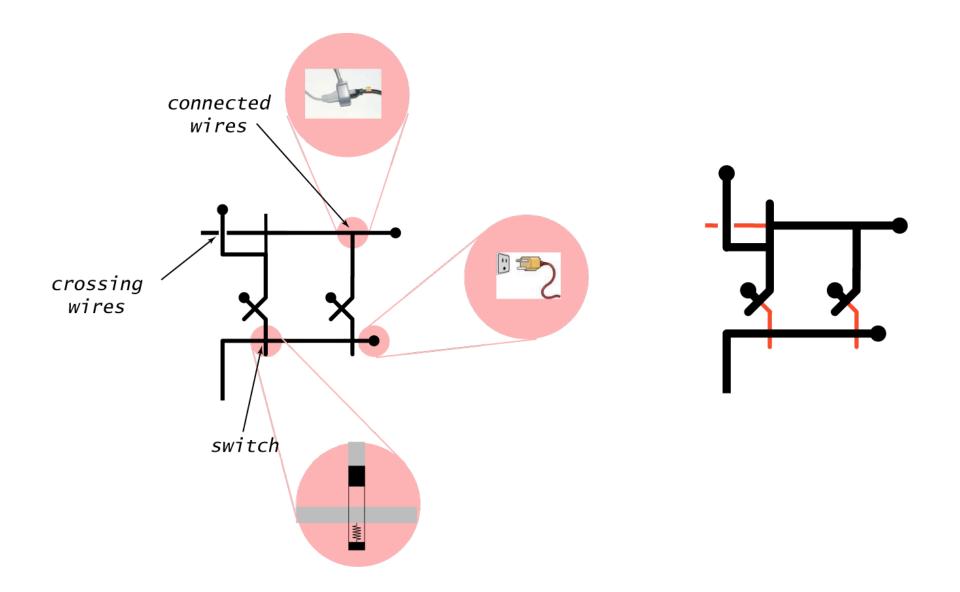




circuit

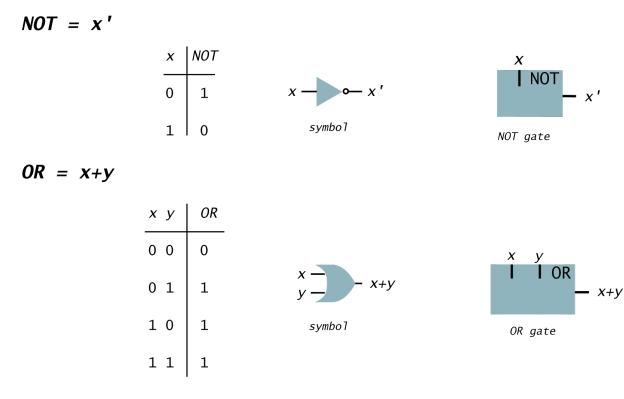


# Circuit Anatomy

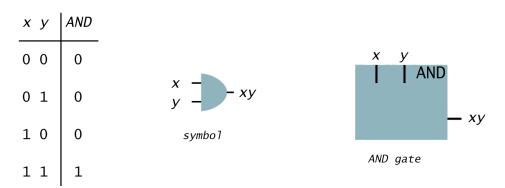


need more "levels of abstraction" to understand circuit behavior

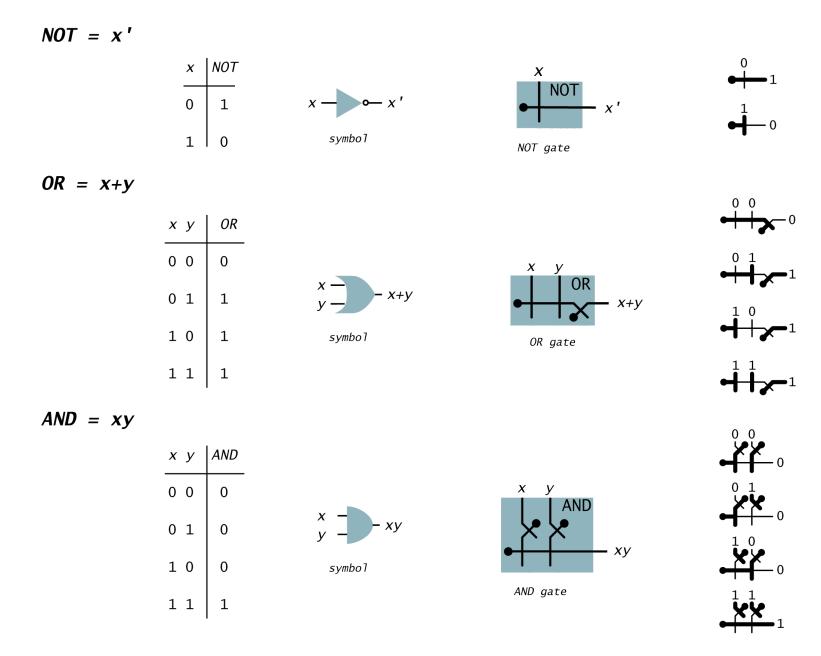
# Second Level of Abstraction: Logic Gates



AND = xy



# Second Level of Abstraction: Logic Gates

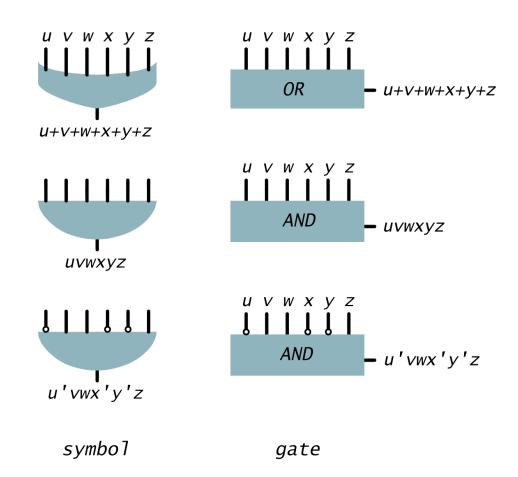


implementations with switches

# Multiway Gates

## Multiway gates.

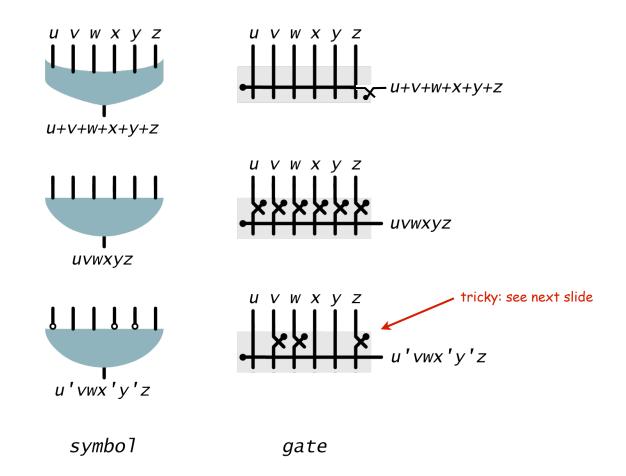
- OR: 1 if any input is 1; 0 otherwise.
- AND: 1 if all inputs are 1; 0 otherwise.
- Generalized: negate some inputs.



# Multiway Gates

## Multiway gates.

- OR: 1 if any input is 1; 0 otherwise.
- AND: 1 if all inputs are 1; 0 otherwise.
- Generalized: negate some inputs.



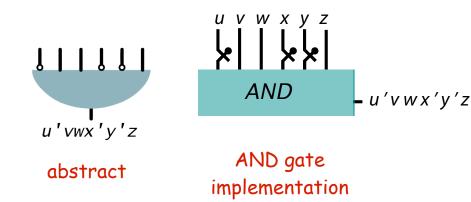
Building blocks (summary)

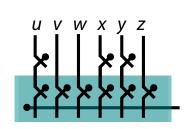
#### Wires

Controlled switches

#### Gates

#### Generalized multiway gates





underlying circuit

simpler version

0 1 1 0 0 1

V

w x y z

value is 1 iff variables with inverters are 1 (and others 0)

'vwx'y'z

1

interpretation:

# Boolean Algebra

# Boolean Algebra

#### History.

- Developed by Boole to solve mathematical logic problems (1847).
- Shannon master's thesis applied it to digital circuits (1937).

"possibly the most important, and also the most famous, master's thesis of the [20th] century" — Howard Gardner

#### Boolean algebra.

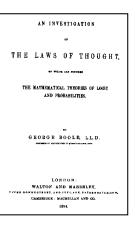
- Boolean variable: value is 0 or 1.
- Boolean function: function whose inputs and outputs are 0, 1.

#### Relationship to circuits.

- Boolean variable: signal.
- Boolean function: circuit.



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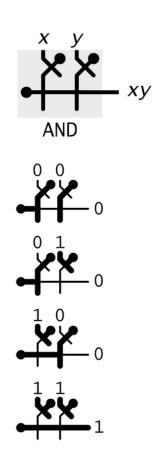
# Truth Table

## Truth table.

- Systematic method to describe Boolean function.
- One row for each possible input combination.
- *n* inputs  $\Rightarrow$   $2^n$  rows.

| X | у | x y |
|---|---|-----|
| 0 | 0 | 0   |
| 0 | 1 | 0   |
| 1 | 0 | 0   |
| 1 | 1 | 1   |

AND truth table



# Truth Table for Functions of 2 Variables

#### Truth table.

• 16 Boolean functions of 2 variables.

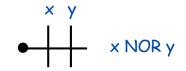
— every 4-bit value represents one

| x | у | ZERO | AND |   | X |   | у | XOR | OR |
|---|---|------|-----|---|---|---|---|-----|----|
| 0 | 0 | 0    | 0   | 0 | 0 | 0 | 0 | 0   | 0  |
| 0 | 1 | 0    | 0   | 0 | 0 | 1 | 1 | 1   | 1  |
| 1 | 0 | 0    | 0   | 1 | 1 | 0 | 0 | 1   | 1  |
| 1 | 1 | 0    | 1   | 0 | 1 | 0 | 1 | 0   | 1  |

truth table for all Boolean functions of 2 variables

| x | у | NOR | EQ | y' |   | <i>x</i> ' |   | NAND | ONE |
|---|---|-----|----|----|---|------------|---|------|-----|
| 0 | 0 | 1   | 1  | 1  | 1 | 1          | 1 | 1    | 1   |
| 0 | 1 | 0   | 0  | 0  | 0 | 1          | 1 | 1    | 1   |
| 1 | 0 | 0   | 0  | 1  | 1 | 0          | 0 | 1    | 1   |
| 1 | 1 | 0   | 1  | 0  | 1 | 0          | 1 | 0    | 1   |

truth table for all Boolean functions of 2 variables



# Truth Table for Functions of 3 Variables

## Truth table.

- 16 Boolean functions of 2 variables.
- 256 Boolean functions of 3 variables.
- $2^{(2^n)}$  Boolean functions of *n* variables!

- every 4-bit value represents one
- every 8-bit value represents one
- every 2<sup>n</sup>-bit value represents one

| x | у | Z. | AND | OR | MAJ | ODD |
|---|---|----|-----|----|-----|-----|
| 0 | 0 | 0  | 0   | 0  | 0   | 0   |
| 0 | 0 | 1  | 0   | 1  | 0   | 1   |
| 0 | 1 | 0  | 0   | 1  | 0   | 1   |
| 0 | 1 | 1  | 0   | 1  | 1   | 0   |
| 1 | 0 | 0  | 0   | 1  | 0   | 1   |
| 1 | 0 | 1  | 0   | 1  | 1   | 0   |
| 1 | 1 | 0  | 0   | 1  | 1   | 0   |
| 1 | 1 | 1  | 1   | 1  | 1   | 1   |

some functions of 3 variables

# Universality of AND, OR, NOT

Fact. Any Boolean function can be expressed using AND, OR, NOT.

- {*AND*, *OR*, *NOT* } are universal.
- **Ex**: XOR(x, y) = xy' + x'y.

| notation   | meaning |
|------------|---------|
| <i>x</i> ' | NOT x   |
| x y        | x AND y |
| x + y      | x OR y  |

Expressing XOR Using AND, OR, NOT

| x | у | <i>x</i> ' | y' | x'y | xy' | x'y + xy' | x XOR y |
|---|---|------------|----|-----|-----|-----------|---------|
| 0 | 0 | 1          | 1  | 0   | 0   | 0         | 0       |
| 0 | 1 | 1          | 0  | 1   | 0   | 1         | 1       |
| 1 | 0 | 0          | 1  | 0   | 1   | 1         | 1       |
| 1 | 1 | 0          | 0  | 0   | 0   | 0         | 0       |

**Exercise.** Show  $\{AND, NOT\}$  are universal. (Hint: DeMorgan's law: (x'y')' = x + y.)

Exercise. Show {NOR} is universal. (Stay tuned for easy proof)

Sum-of-products. Systematic procedure for representing a Boolean function using AND, OR, NOT.

- Form AND term for each 1 in Boolean function.
- OR terms together.

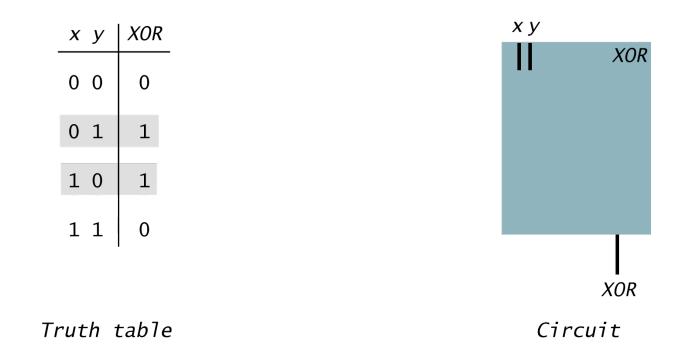
proves that { *AND*, *OR*, *NOT* } are universal

| x | у | Z. | MAJ | x'yz | xy'z | xyz' | xyz | x'yz + xy'z + xyz' + xyz |
|---|---|----|-----|------|------|------|-----|--------------------------|
| 0 | 0 | 0  | 0   | 0    | 0    | 0    | 0   | 0                        |
| 0 | 0 | 1  | 0   | 0    | 0    | 0    | 0   | 0                        |
| 0 | 1 | 0  | 0   | 0    | 0    | 0    | 0   | 0                        |
| 0 | 1 | 1  | 1   | 1    | 0    | 0    | 0   | 1                        |
| 1 | 0 | 0  | 0   | 0    | 0    | 0    | 0   | 0                        |
| 1 | 0 | 1  | 1   | 0    | 1    | 0    | 0   | 1                        |
| 1 | 1 | 0  | 1   | 0    | 0    | 1    | 0   | 1                        |
| 1 | 1 | 1  | 1   | 0    | 0    | 0    | 1   | 1                        |

expressing *MAJ* using sum-of-products

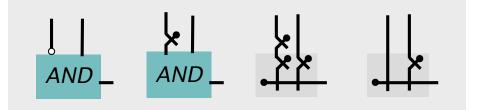
Sum-of-products. XOR.

XOR = x'y + xy'

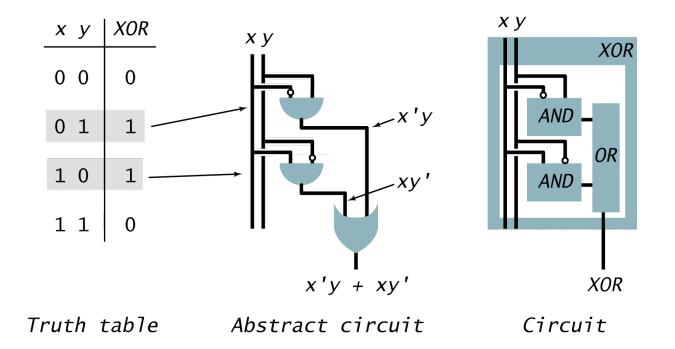


Sum-of-products. XOR.

Key transformation from abstract to real circuit



XOR = x'y + xy'



## Translate Boolean Formula to Boolean Circuit

Example 1. XOR. AND AND \_ XOR = x'y + xy'хy | XOR хy хy XOR 0 0 0 x ' v 0 1 1 1 0 1 xv' 1 1 0 x'y + xy'XOR Truth table Abstract circuit Circuit

$$MAJ = x'yz + xy'z + xyz' + xyz$$

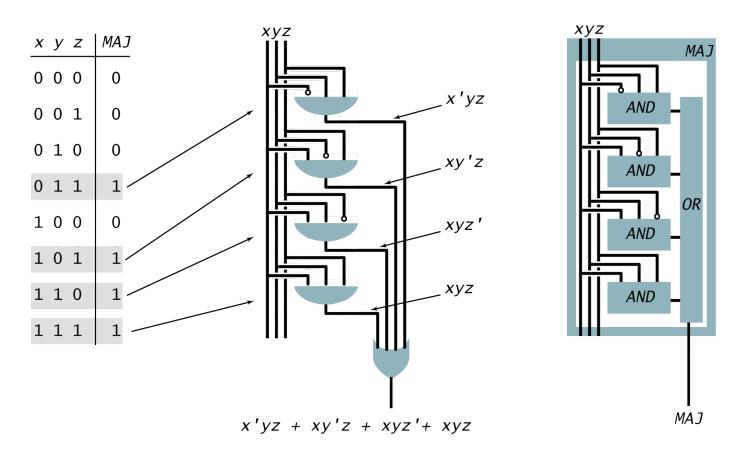


MAJ

Truth table

Circuit

MAJ = x'yz + xy'z + xyz' + xyz

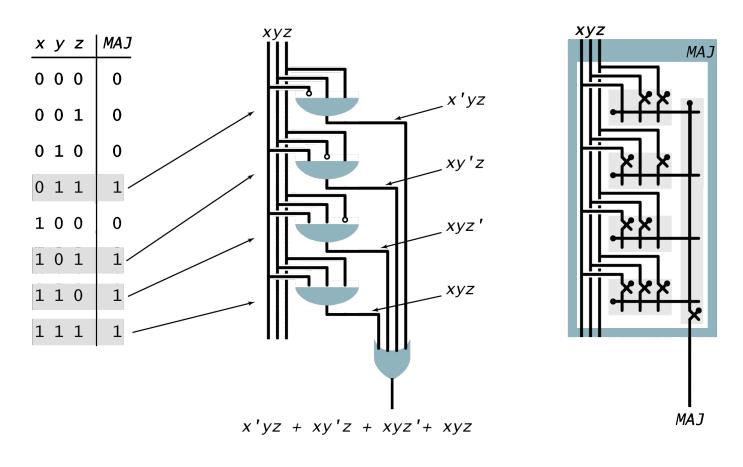


Truth table

Abstract circuit

Circuit

MAJ = x'yz + xy'z + xyz' + xyz

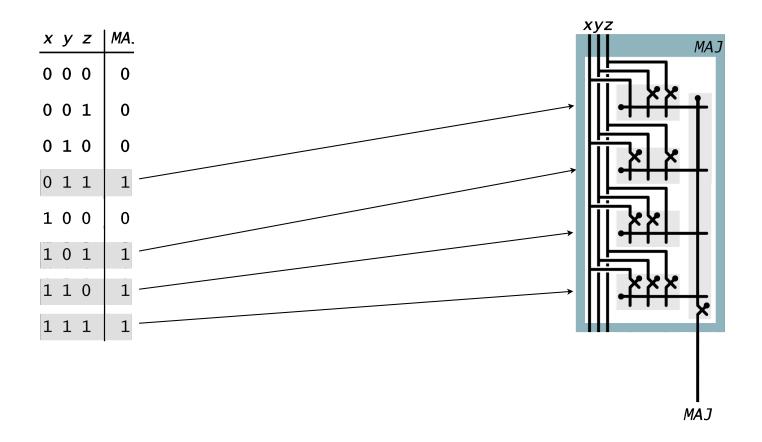


Truth table

Abstract circuit

Circuit

MAJ = x'yz + xy'z + xyz' + xyz



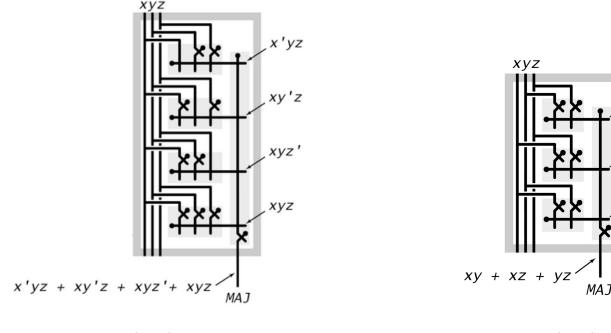


Simplification Using Boolean Algebra

#### Many possible circuits for each Boolean function.

- Sum-of-products not necessarily optimal in:
  - number of switches (space)
  - depth of circuit (time)

**Ex.** MAJ(x, y, z) = x'yz + xy'z + xyz' + xyz = xy + yz + xz.



size = 10, depth = 2

size = 7, depth = 2

VΖ

XΖ

xy

# Combinational Circuit Design: Summary

Problem: Compute the value of a boolean function

### Ingredients.

- AND gates.
- OR gates.
- NOT gates.
- Wire.

### Instructions.

- Step 1: represent input and output signals with Boolean variables.
- Step 2: construct truth table to carry out computation.
- Step 3: derive (simplified) Boolean expression using sum-of products.
- Step 4: transform Boolean expression into circuit.

Bottom line (profound idea):

It is easy to design a circuit to compute ANY boolean function.

Caveat (stay tuned): Circuit might be huge.

Translate Boolean Formula to Boolean Circuit

Example 3. Odd parity

- 1 if odd number of inputs are 1.
- 0 otherwise.

|   |   |    | $\checkmark$ |       |       |       |      |                             |
|---|---|----|--------------|-------|-------|-------|------|-----------------------------|
| X | у | Z. | ODD          | x'y'z | x'yz' | xy'z' | xyz. | x'y'z + x'yz' + xy'z' + xyz |
| 0 | 0 | 0  | 0            | 0     | 0     | 0     | 0    | 0                           |
| 0 | 0 | 1  | 1            | 1     | 0     | 0     | 0    | 1                           |
| 0 | 1 | 0  | 1            | 0     | 1     | 0     | 0    | 1                           |
| 0 | 1 | 1  | 0            | 0     | 0     | 0     | 0    | 0                           |
| 1 | 0 | 0  | 1            | 0     | 0     | 1     | 0    | 1                           |
| 1 | 0 | 1  | 0            | 0     | 0     | 0     | 0    | 0                           |
| 1 | 1 | 0  | 0            | 0     | 0     | 0     | 0    | 0                           |
| 1 | 1 | 1  | 1            | 0     | 0     | 0     | 1    | 1                           |

Expressing ODD using sum-of-products

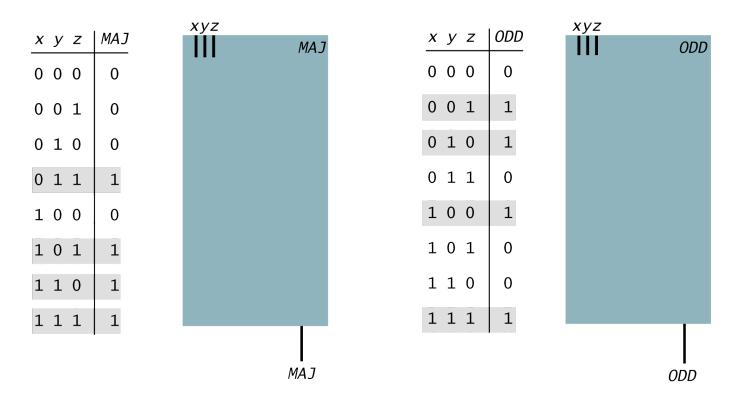
Translate Boolean Formula to Boolean Circuit

Example 3. Odd parity

- 1 if odd number of inputs are 1.
- 0 otherwise.

$$MAJ = x'yz + xy'z + xyz' + xyz$$

$$ODD = x'y'z + x'yz' + xy'z' + xyz$$

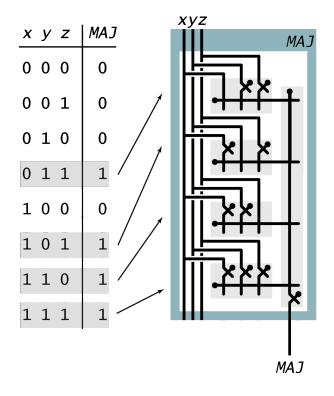


Translate Boolean Formula to Boolean Circuit

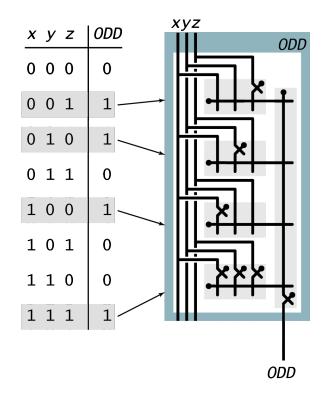
Example 3. Odd parity

- 1 if odd number of inputs are 1.
- 0 otherwise.

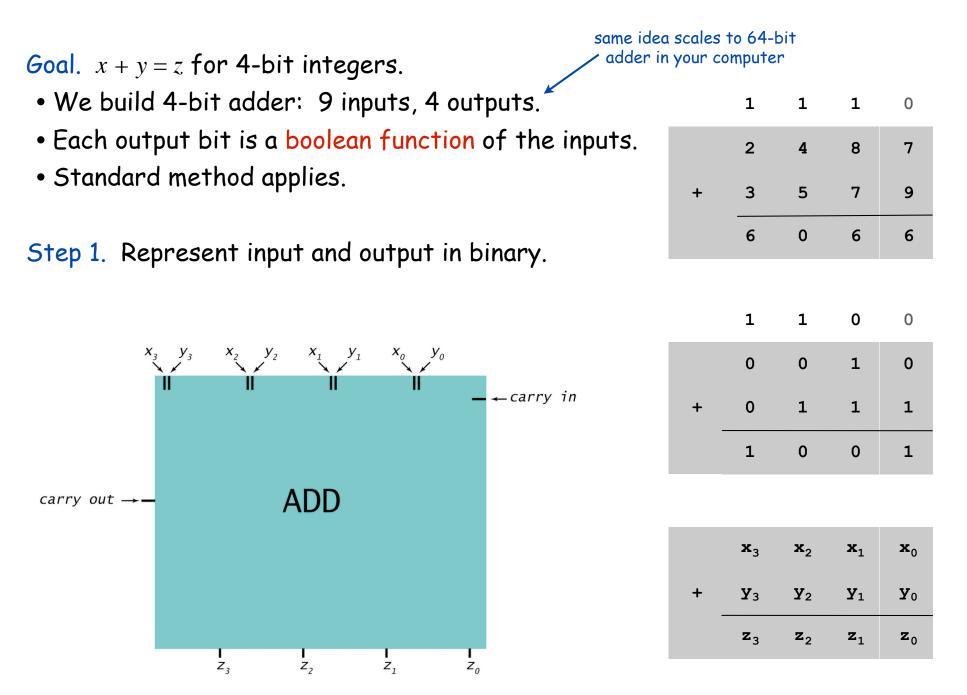
$$MAJ = x'yz + xy'z + xyz' + xyz$$



$$ODD = x'y'z + x'yz' + xy'z' + xyz$$



# Adder Circuit



 $\mathbf{c}_{\mathtt{out}}$ 

+

 $\mathbf{X}_3$ 

**Y**3

Z<sub>3</sub>

 $\mathbf{X}_2$ 

**Y**2

 $\mathbf{Z}_2$ 

 $\mathbf{X}_1$ 

**Y**1

 $\mathbf{Z}_1$ 

|       |                       |                       |                       |                       | 4-bit ad              | lder tru              | th table   | е              |     |                         |         |       |                            |
|-------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|------------|----------------|-----|-------------------------|---------|-------|----------------------------|
| $c_0$ | <i>x</i> <sub>3</sub> | <i>x</i> <sub>2</sub> | <i>x</i> <sub>1</sub> | <i>x</i> <sub>0</sub> | <i>y</i> <sub>3</sub> | <i>y</i> <sub>2</sub> | <i>y</i> 1 | y <sub>0</sub> | Z.3 | <i>z</i> . <sub>2</sub> | $z_{I}$ | $z_0$ |                            |
| 0     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0          | 0              | 0   | 0                       | 0       | 0     |                            |
| 0     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 0          | 1              | 0   | 0                       | 0       | 1     |                            |
| 0     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 1          | 0              | 0   | 0                       | 1       | 0     |                            |
| 0     | 0                     | 0                     | 0                     | 0                     | 0                     | 0                     | 1          | 1              | 0   | 0                       | 1       | 1     | 2 <sup>8+1</sup> = 512 row |
| 0     | 0                     | 0                     | 0                     | 0                     | 0                     | 1                     | 0          | 0              | 0   | 1                       | 0       | 0     |                            |
| •     | •                     | •                     | •                     | •                     | •                     | •                     | •          | •              | •   | •                       | •       | •     |                            |
| 1     | 1                     | 1                     | 1                     | 1                     | 1                     | 1                     | 1          | 1              | 1   | 1                       | 1       | 1     |                            |

#### Goal. x + y = z for 4-bit integers.

- Step 2. [first attempt]
- Build truth table.

- Q. Why is this a bad idea?
- A. 128-bit adder:  $2^{256+1}$  rows  $\gg$  # electrons in universe!

 $\mathbf{C}_{in}$ 

 $\mathbf{x}_0$ 

 $\mathbf{Y}_0$ 

 $\mathbf{z}_{0}$ 

Goal. x + y = z for 4-bit integers.

#### Step 2. Do one bit at a time!

- Build truth table for carry bit.
- Build truth table for summand bit.

| x <sub>i</sub> | y <sub>i</sub> | c <sub>i</sub> | $c_{i+I}$ |
|----------------|----------------|----------------|-----------|
| 0              | 0              | 0              | 0         |
| 0              | 0              | 1              | 0         |
| 0              | 1              | 0              | 0         |
| 0              | 1              | 1              | 1         |
| 1              | 0              | 0              | 0         |
| 1              | 0              | 1              | 1         |
| 1              | 1              | 0              | 1         |
| 1              | 1              | 1              | 1         |

#### carry bit

 $c_0 = 0$  $c_1$  $c_{out}$   $c_3$  $\mathbf{C}_2$  $\mathbf{x}_3$  $\mathbf{X}_2$  $\mathbf{X}_1$  $\mathbf{x}_0$ + **Y**3 **Y**<sub>2</sub>  $\mathbf{Y}_1$  $\mathbf{Y}_0$ **Z**3  $\mathbf{Z}_1$  $\mathbf{Z}_2$  $\mathbf{z}_0$ 

summand bit

| x <sub>i</sub> | y <sub>i</sub> | C <sub>i</sub> | $z_i$ |
|----------------|----------------|----------------|-------|
| 0              | 0              | 0              | 0     |
| 0              | 0              | 1              | 1     |
| 0              | 1              | 0              | 1     |
| 0              | 1              | 1              | 0     |
| 1              | 0              | 0              | 1     |
| 1              | 0              | 1              | 0     |
| 1              | 1              | 0              | 0     |
| 1              | 1              | 1              | 1     |

#### Goal. x + y = z for 4-bit integers.

Step 3. A surprise!

- carry bit is majority function
- summand bit is odd parity function.

| $c_{out}$ | c <sub>3</sub>        | <b>c</b> <sub>2</sub> | $c_1$          | $c_0 = 0$             |
|-----------|-----------------------|-----------------------|----------------|-----------------------|
|           | <b>x</b> <sub>3</sub> | <b>x</b> <sub>2</sub> | $\mathbf{x}_1$ | <b>x</b> <sub>0</sub> |
| +         | <b>У</b> 3            | <b>Y</b> 2            | <b>Y</b> 1     | <b>Y</b> 0            |
|           | <b>z</b> <sub>3</sub> | <b>z</b> <sub>2</sub> | $\mathbf{z}_1$ | <b>z</b> <sub>0</sub> |

carry bit

| x <sub>i</sub> | y <sub>i</sub> | C <sub>i</sub> | <i>c</i> <sub><i>i</i>+1</sub> | MAJ |
|----------------|----------------|----------------|--------------------------------|-----|
| 0              | 0              | 0              | 0                              | 0   |
| 0              | 0              | 1              | 0                              | 0   |
| 0              | 1              | 0              | 0                              | 0   |
| 0              | 1              | 1              | 1                              | 1   |
| 1              | 0              | 0              | 0                              | 0   |
| 1              | 0              | 1              | 1                              | 1   |
| 1              | 1              | 0              | 1                              | 1   |
| 1              | 1              | 1              | 1                              | 1   |

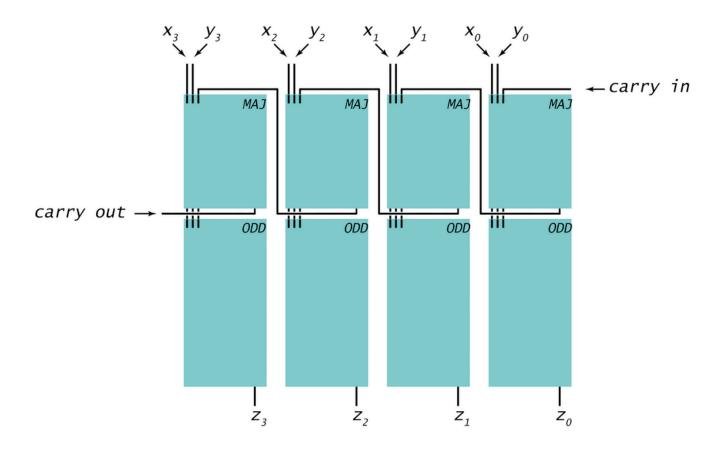
summand bit

| x <sub>i</sub> | y <sub>i</sub> | C <sub>i</sub> | $z_i$ | ODD |
|----------------|----------------|----------------|-------|-----|
| 0              | 0              | 0              | 0     | 0   |
| 0              | 0              | 1              | 1     | 1   |
| 0              | 1              | 0              | 1     | 1   |
| 0              | 1              | 1              | 0     | 0   |
| 1              | 0              | 0              | 1     | 1   |
| 1              | 0              | 1              | 0     | 0   |
| 1              | 1              | 0              | 0     | 0   |
| 1              | 1              | 1              | 1     | 1   |

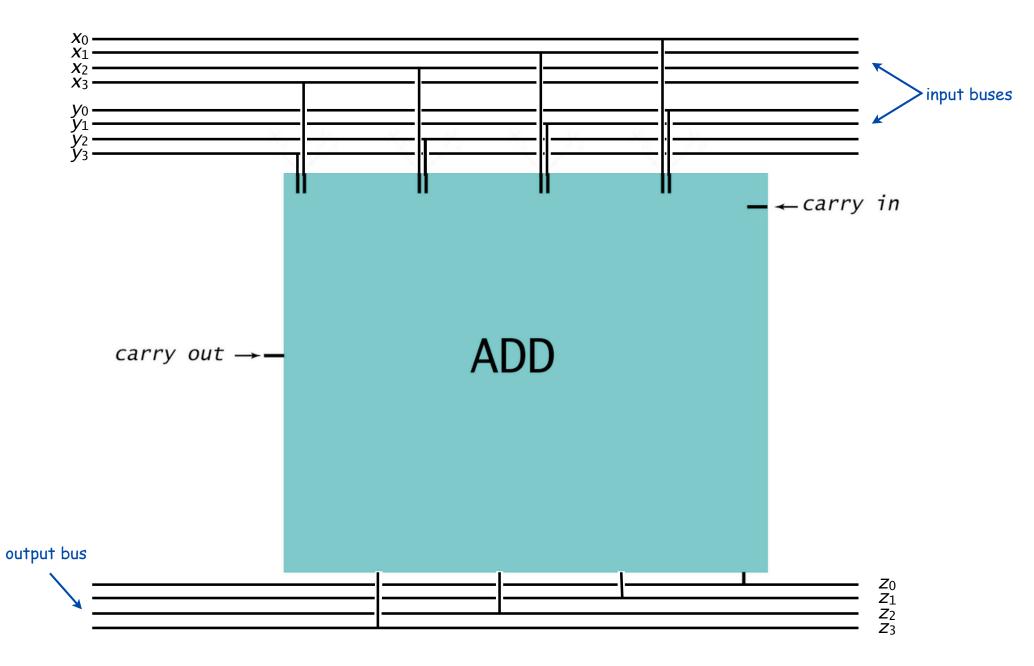
Goal. x + y = z for 4-bit integers.

Step 4.

- Transform Boolean expression into circuit (use known components!).
- Chain together 1-bit adders.
- That's it!

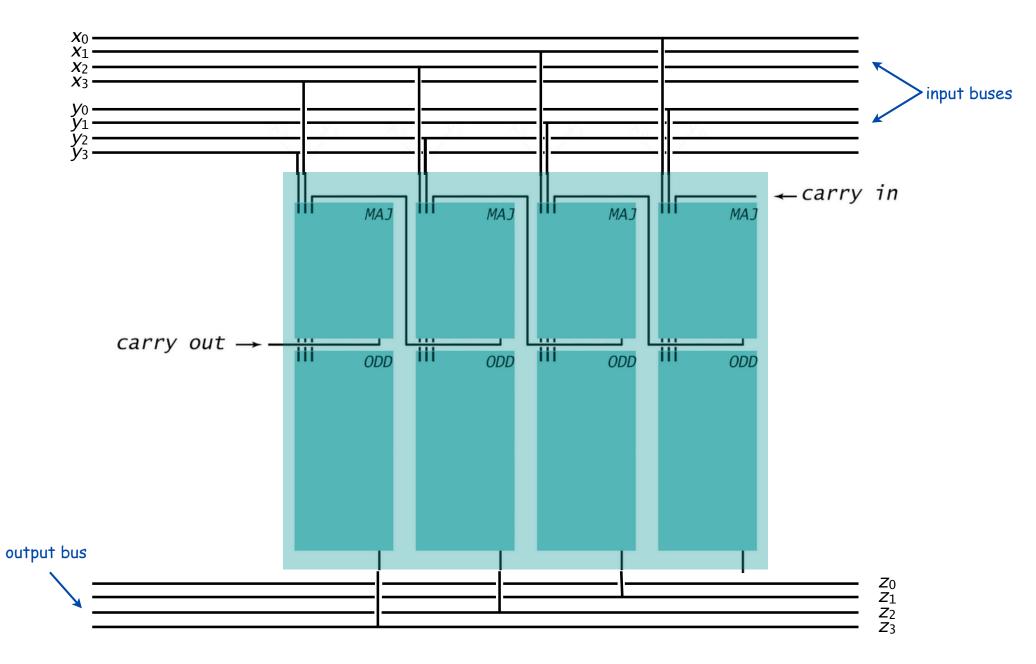


Adder: Interface

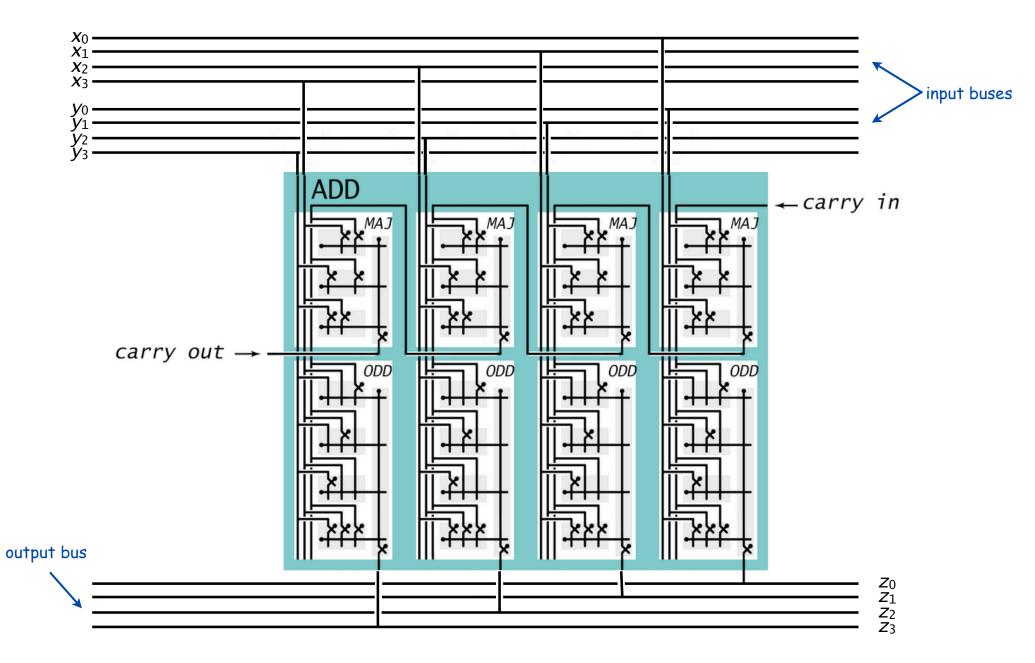


A bus is a group of wires that connect (carry data values) to other components.

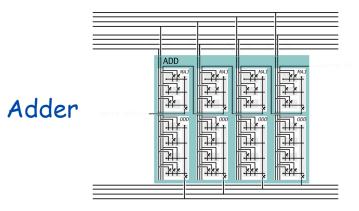
Adder: Component Level View



Adder: Switch Level View



# Useful Combinational Circuits

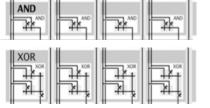


Incrementer (easy, add 0001)

| INCREM | ENT |  |
|--------|-----|--|
|        |     |  |

Bitwise AND, XOR (easy)

Decoder [next slide]



Shifter (clever, but we'll skip details)

Multiplexer [next lecture]

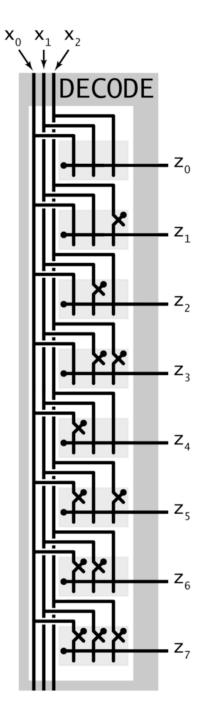
|       |      |                       |      |       |   | ₩¥<br>₩ |
|-------|------|-----------------------|------|-------|---|---------|
|       |      |                       |      |       |   | **      |
| XX XX | XX X | T T T                 | XX X |       | ₩¥<br>₩   | ¥¥      |
|       | XX X |                       |      |       | XX  | *×      |
|       | XX X | <u><u><u></u></u></u> | XX X | IK IK | XX  | *×      |
|       |      |                       |      |       |   |         |
|       | XX X |                       |      |       | 1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1 | ××      |

### Decoder

#### Decoder. [n-bit]

- n address inputs, 2<sup>n</sup> data outputs.
- Addressed output bit is 1; others are 0.
- Compact implementation of n Boolean functions

| $\mathbf{x}_0$ | $\mathbf{x}_1$ | <b>x</b> <sub>2</sub> | z <sub>0</sub> | <b>z</b> 1 | <b>z</b> 2 | <b>z</b> 3 | <b>Z</b> 4 | <b>z</b> 5 | Z6 | <b>Z</b> 7 |
|----------------|----------------|-----------------------|----------------|------------|------------|------------|------------|------------|----|------------|
| 0              | 0              | 0                     | 1              | 0          | 0          | 0          | 0          | 0          | 0  | 0          |
| 0              | 0              | 1                     | 0              | 1          | 0          | 0          | 0          | 0          | 0  | 0          |
| 0              | 1              | 0                     | 0              | 0          | 1          | 0          | 0          | 0          | 0  | 0          |
| 0              | 1              | 1                     | 0              | 0          | 0          | 1          | 0          | 0          | 0  | 0          |
| 1              | 0              | 0                     | 0              | 0          | 0          | 0          | 1          | 0          | 0  | 0          |
| 1              | 0              | 1                     | 0              | 0          | 0          | 0          | 0          | 1          | 0  | 0          |
| 1              | 1              | 0                     | 0              | 0          | 0          | 0          | 0          | 0          | 1  | 0          |
| 1              | 1              | 1                     | 0              | 0          | 0          | 0          | 0          | 0          | 0  | 1          |



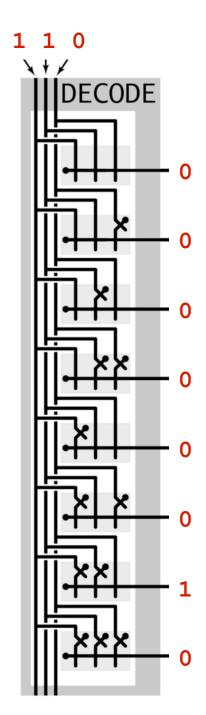
3-bit Decoder

### Decoder

#### Decoder. [n-bit]

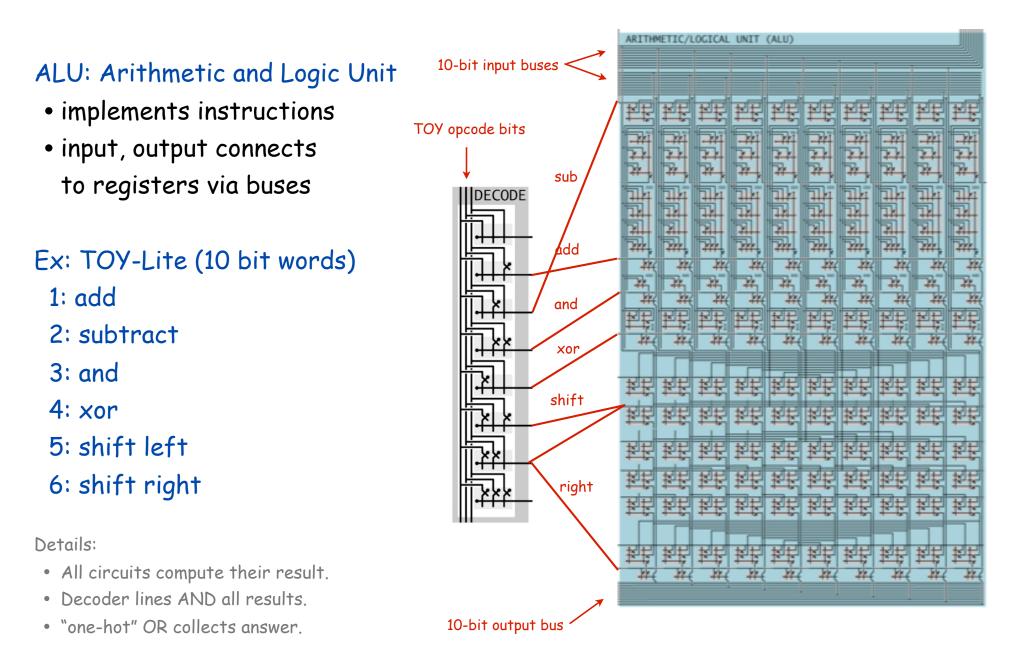
- n address inputs, 2<sup>n</sup> data outputs.
- Addressed output bit is 1; others are 0.
- Compact implementation of n Boolean functions

| $\mathbf{x}_0$ | $\mathbf{x}_1$ | <b>x</b> <sub>2</sub> | <b>z</b> 0 | <b>z</b> 1 | <b>z</b> 2 | <b>z</b> 3 | <b>Z</b> 4 | <b>z</b> 5 | <b>z</b> 6 | <b>Z</b> 7 |
|----------------|----------------|-----------------------|------------|------------|------------|------------|------------|------------|------------|------------|
| 0              | 0              | 0                     | 1          | 0          | 0          | 0          | 0          | 0          | 0          | 0          |
| 0              | 0              | 1                     | 0          | 1          | 0          | 0          | 0          | 0          | 0          | 0          |
| 0              | 1              | 0                     | 0          | 0          | 1          | 0          | 0          | 0          | 0          | 0          |
| 0              | 1              | 1                     | 0          | 0          | 0          | 1          | 0          | 0          | 0          | 0          |
| 1              | 0              | 0                     | 0          | 0          | 0          | 0          | 1          | 0          | 0          | 0          |
| 1              | 0              | 1                     | 0          | 0          | 0          | 0          | 0          | 1          | 0          | 0          |
| 1              | 1              | 0                     | 0          | 0          | 0          | 0          | 0          | 0          | 1          | 0          |
| 1              | 1              | 1                     | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 1          |



3-bit Decoder

# Decoder application: Your computer's ALU!



## Summary

#### Lessons for software design apply to hardware design!

- Interface describes behavior of circuit.
- Implementation gives details of how to build it.

# Layers of abstraction apply with a vengeance!

- On/off.
- Controlled switch. [relay, transistor]
- Gates. [AND, OR, NOT]
- Boolean circuit. [MAJ, ODD]
- Adder.
- Shifter.
- Arithmetic logic unit.
- ...
- TOY machine (stay tuned).
- Your computer.

