

Princeton University
COS 217: Introduction to Programming Systems
A Subset of IA-32 Assembly Language

1. Instruction Operands

1.1. Immediate Operands

Syntax: $\$i$

Semantics: Evaluates to i . Note that i could be a label...

Syntax: $\$label$

Semantics: Evaluates to the memory address denoted by $label$.

1.2. Register Operands

Syntax: $\%r$

Semantics: Evaluates to $\text{reg}[r]$, that is, the contents of register r .

1.3. Memory Operands

Syntax: $disp(\%base, \%index, scale)$

Semantics:

$disp$ is a literal or label.

$base$ is a general purpose register.

$index$ is any general purpose register except EBP.

$scale$ is the literal 1, 2, 4, or 8.

One of $disp$, $base$, or $index$ is required. All other fields are optional.

Evaluates to the contents of memory at a certain address. The address is computed using this formula:

$$disp + \text{reg}[base] + (\text{reg}[index] * scale)$$

The default $disp$ is 0. The default $scale$ is 1. If $base$ is omitted, then $\text{reg}[base]$ evaluates to 0. If $index$ is omitted, then $\text{reg}[index]$ evaluates to 0.

2. Commonly Used Memory Operands

Syntax	Semantics	Description
<i>label</i>	disp: <i>label</i> base: (none) index: (none) scale: (none) mem[0+(0*0)+ <i>label</i>] mem[<i>label</i>]	<p>Direct Addressing. The contents of memory at a certain address. The offset of that address is denoted by <i>label</i>.</p> <p>Often used to access a long, word, or byte in the bss, data, or rodata section.</p>
(% <i>r</i>)	disp: (none) base: <i>r</i> index: (none) scale: (none) mem[reg[<i>r</i>]+(0*0)+0] mem[reg[<i>r</i>]]	<p>Indirect Addressing. The contents of memory at a certain address. The offset of that address is the contents of register <i>r</i>.</p> <p>Often used to access a long, word, or byte in the stack section.</p>
<i>i</i> (% <i>r</i>)	disp: <i>i</i> base: <i>r</i> index: (none) scale: (none) mem[reg[<i>r</i>]+(0*0)+ <i>i</i>] mem[reg[<i>r</i>]+ <i>i</i>]	<p>Base-Pointer Addressing. The contents of memory at a certain address. The offset of that address is the sum of <i>i</i> and the contents of register <i>r</i>.</p> <p>Often used to access a long, word, or byte in the stack section.</p>
<i>label</i> (% <i>r</i>)	disp: <i>label</i> base: <i>r</i> index: (none) scale: (none) mem[reg[<i>r</i>]+(0*0)+ <i>label</i>] mem[reg[<i>r</i>]+ <i>label</i>]	<p>Indexed Addressing. The contents of memory at a certain address. The offset of that address is the sum of the address denoted by <i>label</i> and the contents of register <i>r</i>.</p> <p>Often used to access an array of bytes (characters) in the bss, data, or rodata section.</p>
<i>label</i> (,% <i>r</i> , <i>i</i>)	disp: <i>label</i> base: (none) index: <i>r</i> scale: <i>i</i> mem[0+(reg[<i>r</i>]* <i>i</i>)+ <i>label</i>] mem[(reg[<i>r</i>]* <i>i</i>)+ <i>label</i>]	<p>Indexed Addressing. The contents of memory at a certain address. The offset of that address is the sum of the address denoted by <i>label</i>, and the contents of register <i>r</i> multiplied by <i>i</i>.</p> <p>Often used to access an array of longs or words in the bss, data, or rodata section.</p>

3. Assembler Mnemonics

Key:

src: a source operand
dest: a destination operand
I: an immediate operand
R: a register operand
M: a memory operand
label: a label operand

For each instruction, at most one operand can be a memory operand.

3.1. Data Transfer Mnemonics

Syntax	Semantics (expressed using C-like syntax)	Description
<code>mov{1,w,b} srcIRM, destRM</code>	$dest = src;$	Move. Copy <i>src</i> to <i>dest</i> . Flags affected: None
<code>push{1,w} srcIRM</code>	$reg[ESP] = reg[ESP] - \{4,2\};$ $mem[reg[ESP]] = src;$	Push. Push <i>src</i> onto the stack. Flags affected: None
<code>pop{1,w} destRM</code>	$dest = mem[reg[ESP]];$ $reg[ESP] = reg[ESP] + \{4,2\};$	Pop. Pop from the stack into <i>dest</i> . Flags affected: None
<code>lea{1,w} srcM, destR</code>	$dest = \&src;$	Load Effective Address. Assign the address of <i>src</i> to <i>dest</i> . Flags affected: None
<code>cld</code>	$reg[EDX:EAX] = reg[EAX];$	Convert Long to Double Register. Sign extend the contents of register EAX into the register pair EDX:EAX, typically in preparation for <code>idivl</code> . Flags affected: None
<code>cwtd</code>	$reg[DX:AX] = reg[AX];$	Convert Word to Double Register. Sign extend the contents of register AX into the register pair DX:AX, typically in preparation for <code>idivw</code> . Flags affected: None
<code>cbtw</code>	$reg[AX] = reg[AL];$	Convert Byte to Word. Sign extend the contents of register AL into register AX, typically in preparation for <code>idivb</code> . Flags affected: None
<code>leave</code>	Equivalent to: <code>movl %ebp, %esp</code> <code>popl %ebp</code>	Pop a stack frame in preparation for leaving a function. Flags affected: None

3.2. Arithmetic Mnemonics

Syntax	Semantics (expressed using C-like syntax)	Description
<code>add{1,w,b} srcIRM, destRM</code>	$dest = dest + src;$	Add. Add <i>src</i> to <i>dest</i> . Flags affected: O, S, Z, A, C, P
<code>adc{1,w,b} srcIRM, destRM</code>	$dest = dest + src + C;$	Add with Carry. Add <i>src</i> and the carry flag to <i>dest</i> . Flags affected: O, S, Z, A, C, P
<code>sub{1,w,b} srcIRM, destRM</code>	$dest = dest - src;$	Subtract. Subtract <i>src</i> from <i>dest</i> . Flags affected: O, S, Z, A, C, P
<code>inc{1,w,b} destRM</code>	$dest = dest + 1;$	Increment. Increment <i>dest</i> . Flags affected: O, S, Z, A, P
<code>dec{1,w,b} destRM</code>	$dest = dest - 1;$	Decrement. Decrement <i>dest</i> . Flags affected: O, S, Z, A, P

<code>neg{1,w,b} destRM</code>	<code>dest = -dest;</code>	Negate. Negate <i>dest</i> . Flags affected: O, S, Z, A, C, P
<code>imull srcRM</code>	<code>reg[EDX:EAX] = reg[EAX]*src;</code>	Signed Multiply. Multiply the contents of register EAX by <i>src</i> , and store the product in registers EDX:EAX. Flags affected: O, S, Z, A, C, P
<code>imulw srcRM</code>	<code>reg[DX:AX] = reg[AX]*src;</code>	Signed Multiply. Multiply the contents of register AX by <i>src</i> , and store the product in registers DX:AX. Flags affected: O, S, Z, A, C, P
<code>imulb srcRM</code>	<code>reg[AX] = reg[AL]*src;</code>	Signed Multiply. Multiply the contents of register AL by <i>src</i> , and store the product in AX. Flags affected: O, S, Z, A, C, P
<code>idivl srcRM</code>	<code>reg[EAX] = reg[EDX:EAX]/src;</code> <code>reg[EDX] = reg[EDX:EAX]%src;</code>	Signed Divide. Divide the contents of registers EDX:EAX by <i>src</i> , and store the quotient in register EAX and the remainder in register EDX. Flags affected: O, S, Z, A, C, P
<code>idivw srcRM</code>	<code>reg[AX] = reg[DX:AX]/src;</code> <code>reg[DX] = reg[DX:AX]%src;</code>	Signed Divide. Divide the contents of registers DX:AX by <i>src</i> , and store the quotient in register AX and the remainder in register DX. Flags affected: O, S, Z, A, C, P
<code>idivb srcRM</code>	<code>reg[AL] = reg[AX]/src;</code> <code>reg[AH] = reg[AX]%src;</code>	Signed Divide. Divide the contents of register AX by <i>src</i> , and store the quotient in register AL and the remainder in register AH. Flags affected: O, S, Z, A, C, P
<code>mull srcRM</code>	<code>reg[EDX:EAX] = reg[EAX]*src;</code>	Unsigned Multiply. Multiply the contents of register EAX by <i>src</i> , and store the product in registers EDX:EAX. Flags affected: O, S, Z, A, C, P
<code>mulw srcRM</code>	<code>reg[DX:AX] = reg[AX]*src;</code>	Unsigned Multiply. Multiply the contents of register AX by <i>src</i> , and store the product in registers DX:AX. Flags affected: O, S, Z, A, C, P
<code>mulb srcRM</code>	<code>reg[AX] = reg[AL]*src;</code>	Unsigned Multiply. Multiply the contents of register AL by <i>src</i> , and store the product in AX.
<code>divl srcRM</code>	<code>reg[EAX] = reg[EDX:EAX]/src;</code> <code>reg[EDX] = reg[EDX:EAX]%src;</code>	Unsigned Divide. Divide the contents of registers EDX:EAX by <i>src</i> , and store the quotient in register EAX and the remainder in register EDX. Flags affected: O, S, Z, A, C, P
<code>divw srcRM</code>	<code>reg[AX] = reg[DX:AX]/src;</code> <code>reg[DX] = reg[DX:AX]%src;</code>	Unsigned Divide. Divide the contents of registers DX:AX by <i>src</i> , and store the quotient in register AX and the remainder in register DX. Flags affected: O, S, Z, A, C, P
<code>divb srcRM</code>	<code>reg[AL] = reg[AX]/src;</code> <code>reg[AH] = reg[AX]%src;</code>	Unsigned Divide. Divide the contents of register AX by <i>src</i> , and store the quotient in register AL and the remainder in register AH. Flags affected: O, S, Z, A, C, P

3.3. Bitwise Mnemonics

Syntax	Semantics (expressed using C-like syntax)	Description
<code>and{1,w,b} srcIRM, destRM</code>	<code>dest = dest & src;</code>	And. Bitwise and <i>src</i> into <i>dest</i> . Flags affected: O, S, Z, A, C, P
<code>or{1,w,b} srcIRM, destRM</code>	<code>dest = dest src;</code>	Or. Bitwise or <i>src</i> into <i>dest</i> . Flags affected: O, S, Z, A, C, P

<code>xor{1,w,b} srcIRM, destRM</code>	<code>dest = dest ^ src;</code>	Exclusive Or. Bitwise exclusive or <i>src</i> into <i>dest</i> . Flags affected: O, S, Z, A, C, P
<code>not{1,w,b} destRM</code>	<code>dest = ~dest;</code>	Not. Bitwise not <i>dest</i> . Flags affected: None
<code>sal{1,w,b} srcIR, destRM</code>	<code>dest = dest << src;</code>	Shift Arithmetic Left. Shift <i>dest</i> to the left <i>src</i> bits, filling with zeros. Flags affected: O, S, Z, A, C, P
<code>sar{1,w,b} srcIR, destRM</code>	<code>dest = dest >> src;</code>	Shift Arithmetic Right. Shift <i>dest</i> to the right <i>src</i> bits, sign extending the number. Flags affected: O, S, Z, A, C, P
<code>shl{1,w,b} srcIR, destRM</code>	(Same as <code>sal</code>)	Shift Left. (Same as <code>sal</code>). Flags affected: O, S, Z, A, C, P
<code>shr{1,w,b} srcIR, destRM</code>	(Same as <code>sar</code>)	Shift Right. Shift <i>dest</i> to the right <i>src</i> bits, filling with zeros. Flags affected: O, S, Z, A, C, P

3.4. Control Transfer Mnemonics

Syntax	Semantics (expressed using C-like syntax)	Description
<code>cmp{1,w,b} srcIRM1,srcRM2</code>	<code>reg[EFLAGS] = srcRM2 comparedwith srcIRM1</code>	Compare. Compare <i>src2</i> with <i>src1</i> , and set the flags in the EFLAGS register accordingly. Flags affected: O, S, Z, A, C, P
<code>jmp label</code>	<code>reg[EIP] = label;</code>	Jump. Jump to <i>label</i> . Flags affected: None
<code>j{e,ne} label</code>	<code>if (reg[EFLAGS] appropriate) reg[EIP] = label;</code>	Conditional Jump. Jump to <i>label</i> iff the flags in the EFLAGS register indicate an equality or inequality (respectively) relationship between the most recently compared numbers. Flags affected: None
<code>j{1,le,g,ge} label</code>	<code>if (reg[EFLAGS] appropriate) reg[EIP] = label;</code>	Signed Conditional Jump. Jump to <i>label</i> iff the condition codes in the EFLAGS register indicate a less than, less than or equal to, greater than, or greater than or equal to (respectively) relationship between the most recently compared numbers. Flags affected: None
<code>j{b,be,a,ae} label</code>	<code>if (reg[EFLAGS] appropriate) reg[EIP] = label;</code>	Unsigned Conditional Jump. Jump to <i>label</i> iff the condition codes in the EFLAGS register indicate a below, below or equal to, above, or above or equal to (respectively) relationship between the most recently compared numbers. Flags affected: None
<code>call label</code>	<code>reg[ESP] = reg[ESP] - 4; mem[reg[ESP]] = reg[EIP]; reg[EIP] = label;</code>	Call. Call the function that begins at <i>label</i> . Flags affected: None
<code>call *srcR</code>	<code>reg[ESP] = reg[ESP] - 4; mem[reg[ESP]] = reg[EIP]; reg[EIP] = reg[srcR];</code>	Call. Call the function whose address is in <i>src</i> . Flags affected: None
<code>ret</code>	<code>reg[EIP] = mem[reg[ESP]]; reg[ESP] = reg[ESP] + 4;</code>	Return. Return from the current function. Flags affected: None
<code>int srcIRM</code>	Generate interrupt number <i>src</i>	Interrupt. Generate interrupt number <i>src</i> . Flags affected: None

4. Assembler Directives

Syntax	Description
<code>label:</code>	Record the fact that <i>label</i> marks the current location within the current section
<code>.section ".sectionname"</code>	Make the <i>sectionname</i> section the current section
<code>.skip n</code>	Skip <i>n</i> bytes of memory in the current section
<code>.align n</code>	Skip as many bytes of memory in the current section as necessary so the current location is evenly divisible by <i>n</i>
<code>.byte bytevalue1, bytevalue2, ...</code>	Allocate one byte of memory containing <i>bytevalue1</i> , one byte of memory containing <i>bytevalue2</i> , ... in the current section
<code>.word wordvalue1, wordvalue2, ...</code>	Allocate two bytes of memory containing <i>wordvalue1</i> , two bytes of memory containing <i>wordvalue2</i> , ... in the current section
<code>.long longvalue1, longvalue2, ...</code>	Allocate four bytes of memory containing <i>longvalue1</i> , four bytes of memory containing <i>longvalue2</i> , ... in the current section
<code>.ascii "string1", "string2", ...</code>	Allocate memory containing the characters from <i>string1</i> , <i>string2</i> , ... in the current section
<code>.asciz "string1", "string2", ...</code>	Allocate memory containing <i>string1</i> , <i>string2</i> , ..., where each string is '\0' terminated, in the current section
<code>.string "string1", "string2", ...</code>	(Same as <code>.asciz</code>)
<code>.globl label1, label2, ...</code>	Mark <i>label1</i> , <i>label2</i> , ... so they are accessible by code generated from other source code files
<code>.equ name, expr</code>	Define <i>name</i> as a symbolic alias for <i>expr</i>
<code>.lcomm label, n [,align]</code>	Allocate <i>n</i> bytes, marked by <i>label</i> , in the bss section [and align the bytes on an <i>align</i> -byte boundary]
<code>.comm label, n [,align]</code>	Allocate <i>n</i> bytes, marked by <i>label</i> , in the bss section, mark label so it is accessible by code generated from other source code files [and align the bytes on an <i>align</i> -byte boundary]
<code>.type label,@function</code>	Mark <i>label</i> so the linker knows that it denotes the beginning of a function

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