

# COS 471A, COS 471B/ELE 375 Assignment #2

Due Oct 21st at 5pm, 2005

Fall 2005, Princeton University

## **Homework Submission Instructions:**

Your course enrollment (COS 471A, COS 471B/ELE 375) should be listed with your name on the front page of your submission. Submit your assignment using the envelope outside CS 004. State all assumptions. **LATE SUBMISSIONS:** Record the date and time of your submission.

## **Do the following:**

1. What is the worst case delay of a 1-level 5-bit carry look ahead adder and ripple-carry adder (in terms of # of gate delays)? Which set of input combinations cause the worst case delay? Elaborate with reasons.
2. Design a 6-bit Shifter (left & right logical and arithmetic) which allows a maximum shift of 4-bits. You do not need to implement any other instructions.
3. Prove that a sign extension of any length correctly maintains the value of all 2's complement numbers.
4. Why is the 2's complement representation used most often? Give an example of overflow when:
  - 2 positive numbers are added
  - 2 negative numbers are added
  - A-B where B is a negative number
5. (Similar to P&H 2nd ed, 5.12) Consider the following idea: Let's modify the instruction set architecture and remove the ability to specify an offset for memory access instructions. Specifically, all load-store instructions with nonzero offsets would become pseudoinstructions and would be implemented using two instructions. For example:

```
addi $at, $t1, 104 # add the offset to a temporary
lw   $t0, $at      # new way of doing lw $t0, 104($t1)
```

What changes would you make to the single-cycle datapath and control if this simplified architecture were to be used? Feel free to use the figure on the next page.

6. (Similar to P&H 3rd ed, 5.35) Consider a change to the multiple-cycle implementation presented in lecture that alters the register file so that it has only one read port. Neatly describe (via a diagram) any additional changes that will need to be made to the datapath in order to support this modification. Describe (via another diagram) the changes to the finite state machine necessary to make the instructions (LW, SW, R-type, BEQ, J) work with your new datapath.

